KUMARAGURU COLLEGE OF TECHNOLOGY, COIMBATORE - 641049
M.E. APPLIED ELECTRONICS
CURRICULUM 2013

SEMESTER – I

Code No.	Course Title	L	T	P	C
Theory					
P13MAT108	Applied Algebra	3	1	0	4
P13AET101	Advanced Digital System Design	3	1	0	4
P13AET102	VLSI Design Techniques	3	0	0	3
P13AET103	Advanced Signal Processing	3	1	0	4
P13AET104	Embedded Systems	3	0	0	3
ET1***	Elective I	3	0	0	3
Practical					
P13AEP101	Embedded Systems Laboratory	0	0	3	1
Total					**22**

SEMESTER – II

Code No.	Course Title	L	T	P	C
Theory					
P13AET201	Analog Integrated Circuit Design	3	1	0	4
P13AET202	Advanced Control Engineering	3	0	0	3
P13AET203	ASIC Design	3	0	0	3
ET2***	Elective II	3	0	0	3
ET3***	Elective III	3	0	0	3
ET4***	Elective IV	3	0	0	3
Practical					
P13AEP201	VLSI Laboratory	0	0	3	1
Total					**20**

SEMESTER – III

Code No.	Course Title	L	T	P	C
Theory					
ET5***	Elective V	3	0	0	3
ET6***	Elective VI	3	0	0	3
ET7***	Elective VII	3	0	0	3
Practical					
P13AEP301	Project Work (Phase I)	0	0	12	6
Total					**15**

SEMESTER – IV

Code No.	Course Title	L	T	P	C
P13AEP401	Project Work (Phase II)	0	0	24	12
Total					**12**

TOTAL CREDITS : 69

M.E. APPLIED ELECTRONICS
ELECTIVES

Code No.	Course Title	L	T	P	C
P13AETE01	Advanced Digital Image Processing	3	0	0	3
P13AETE02	Neural Networks and Applications	3	0	0	3
P13AETE03	Low Power VLSI Design	3	0	0	3
P13AETE04	DSP Integrated Circuits	3	0	0	3
P13AETE05	Advanced Computer Architecture	3	0	0	3
P13AETE06	Hardware Software Co-Design	3	0	0	3
P13AETE07	Design and Analysis of Algorithms	3	0	0	3
P13AETE08	Soft Computing	3	0	0	3
P13COTE09	Internetworking Multimedia	3	0	0	3
P13AETE09	DSP Processor Architecture and Programming	3	0	0	3
P13COTE11	High Performance Communication Networks	3	0	0	3
P13COTE12	High Speed Switching Architecture	3	0	0	3
P13AETE10	VLSI Signal Processing	3	0	0	3
P13AETE11	Analog VLSI Design	3	0	0	3
P13AETE12	Computer Aided Design of VLSI Circuits	3	0	0	3
P13AETE13	Stochastic Models and Simulation	3	0	0	3
P13AETE14	Mobile Computing	3	0	0	3
P13AETE15	Cellular and Mobile Communication	3	0	0	3
P13AETE16	Visualization Techniques	3	0	0	3
P13AETE17	Machine Vision	3	0	0	3
P13AETE18	Machine learning	3	0	0	3
P13AETE19	Pattern Recognition and Artificial Intelligence	3	0	0	3
P13AETE20	Image Processing and Pattern Recognition	3	0	0	3
P13AETE21	Image and Video processing	3	0	0	3
P13AETE22	Mixed Signal VLSI Design	3	0	0	3
P13AETE23	VLSI Testing and Testability	3	0	0	3
P13AETE24	Power Electronics	3	0	0	3
P13AETE25	Data Converters	3	0	0	3
P13AETE26	Synthesis and Optimization of Digital Circuits	3	0	0	3
P13AETE27	Virtual Instrumentation	3	0	0	3
P13AETE28	Wavelets and Multiresolution Processing	3	0	0	3
P13AETE29	Multirate Signal Processing	3	0	0	3
P13AETE30	Multimedia Compression Techniques	3	0	0	3
P13COTE23	Speech and Audio Signal Processing	3	0	0	3
P13AETE31	Robotics	3	0	0	3
P13AETE32	Microelectromechanical Systems	3	0	0	3
P13AETE33	Advanced Processors	3	0	0	3
P13AETE34	Process Control	3	0	0	3
P13AETE35	Embedded Systems in Automotive Applications	3	0	0	3
P13AETE36	Advanced Embedded Development	3	0	0	3
P13AETE37	System Modeling and Simulation	3	0	0	3
P13COTE24	Research Methodology	3	0	0	3
	Special Elective	3	0	0	3

P13MAT108 APPLIED ALGEBRA

L	T	P	C
3	1	0	4

UNIT I LINEAR EQUATIONS **09**

System of linear equations - Row reduction & Echelon forms -Vector equations - Matrix equation Ax=b - Solution sets of linear systems: Direct and Iterative methods - Application of linear systems - Linear Independence.

UNIT II MATRIX ALGEBRA **09**

Matrix operations - Inverse of a matrix - Characteristics of invertible matrices - Partitioned matrices -Matrix factorizations - Subspaces of Rn - Dimension & rank - Introduction to determinants - Properties of determinants - Cramer's rule.

UNIT III VECTOR SPACES **09**

Vector spaces & subspaces - Null spaces, column spaces & linear transformations - Linearly independent sets; Bases - Coordinate systems - Dimension of a vector space – Rank - Change of basis- Eigen values & Eigen vectors - Characteristic equation –Diagonalization of symmetric matrices - Eigenvectors & linear transformations - Complex Eigen values - Applications to differential equations.

UNIT IV ORTHOGONALITY AND LEAST SQUARES **09**

Inner product, Length and Orthogonality - Orthogonal sets - Orthogonal projections –Gram - Schmidt process - Inner product spaces - Applications of inner product spaces - Quadratic forms - Singular value decomposition - Applications to image processing.

UNIT V RANDOM VARIABLES **09**

One-dimensional Random Variables – Moments and MGF – Binomial, Poisson, Geometric, Exponential and Normal distributions – Two-dimensional Random Variables – Marginal and Conditional distribution – Covariance and Correlation coefficient.

L:45; T:15
TOTAL: 60

REFERENCES

1. *David C. Lay, "**Linear Algebra and its Applications**", Pearson Education Asia, New Delhi, 2003*
2. *Gilbert Strang, "**Linear Algebra and its Applications**", Brooks/Cole Ltd., New Delhi, Third Edition,2003*
3. *Seymour Lipschutz , Marc Lipson, "**Schaum's Outline of Linear Algebra**", McGraw Hill Trade; New Delhi, Third Edition, 2000*
4. *Howard A. Anton , "**Elementary Linear Algebra**", John Wiley & Sons, Singapore, Eighth*
5. *Veerarajan. T., " **Probability and Random Process**", Tata McGraw Hill,2008*

P13AET101 ADVANCED DIGITAL SYSTEM DESIGN

L	T	P	C
3	1	0	4

UNIT I SYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 09

Analysis of Clocked Synchronous Sequential Circuits - Modeling, state table reduction, state assignment, Design of Synchronous Sequential Networks, Design of iterative circuits - ASM chart - ASM realization.

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 09

Analysis of Asynchronous Sequential Circuits - Races in ASC – Primitive Flow Table - Flow Table Reduction Techniques, State Assignment Problem and the Transition Table – Design of ASC – Static and Dynamic Hazards – Essential Hazards.

UNIT III SYSTEM DESIGN USING PLDS 09

Programmable Logic Devices (PLDs): Programmable Read Only Memory (PROM) - Programmable Logic Array (PLA) - Programmable Array Logic (PAL) – Design of combinational circuits using PLDs - Programmable Logic Architectures – PAL16L8 – PAL16R4 – PAL22V10 – Design of sequential circuits using PAL16R4 – Complex PLDs (CPLDs)

UNIT IV INTRODUCTION TO VHDL 09

Design flow - VHDL Code Structure – Library, Entity, Architecture - Behavioral, Data flow and Structural modeling - Data Types - Operators and Attributes – Signals and Variables - Concurrent and Sequential Code – Packages and Components – Subprograms: Functions and Procedures – Design Examples - Test Benches.

UNIT V LOGIC CIRCUIT TESTING AND TESTABLE DESIGN 09

Digital logic circuit testing - Fault models - Combinational logic circuit testing - Sequential logic circuit testing-Design for Testability - Built-in Self-test, Board and System Level Boundary Scan. Case Study: Traffic Light Controller

L:45; T:15
TOTAL: 60

REFERENCES

1. *Donald G. Givone,* ***"Digital principles and Design",*** *Tata McGraw Hill, 2002.*
2. *Nelson, V.P., Nagale, H.T., Carroll, B.D., and Irwin, J.D.,* ***"Digital Logic Circuit Analysis and Design",*** *Prentice Hall International, Inc., New Jersey, 1995*
3. *Volnei A. Pedroni,* ***"Circuit Design with VHDL",*** *MIT Press, 2010.*
4. *John M. Yarbrough, "****Digital Logic Applications and Design****", Cengage Learning India Private Limited, New Delhi, 1997.*
5. *Charles H Roth,* ***"Digital Systems Design Using VHDL,"*** *Thomson Asia. 2004.*
6. *Parag K Lala,* ***"Digital Circuit Testing and Testability",*** *Academic Press, 1997*

P13AET102 VLSI DESIGN TECHNIQUES

L	T	P	C
3	0	0	3

UNIT I MOS TRANSISTOR THEORY AND PROCESS TECHNOLOGY 09

NMOS and PMOS transistors, Threshold voltage - Body effect - Design Equations - Second order effects - MOS models and small signal AC characteristics - Basic CMOS Technology- n-well, p-well, twin-tub, SOI process.

UNIT II INVERTERS AND LOGIC GATES 09

NMOS and CMOS Inverters, Stick diagram, Inverter ratio, DC and transient characteristics, NMOS and CMOS switching speed, Super buffers, Transmission gates, pass transistors, CMOS logic structures - static and dynamic CMOS design, Clocked CMOS logic – Pre-charged domino CMOS logic.

UNIT III CIRCUIT CHARACTERISATION AND PERFORMANCE ESTIMATION 09

Resistance, Capacitance and Inductance estimation, Inverter switching characteristics – fall time, rise time, propagation delay - CMOS - Gate transistor sizing, power dissipation.

UNIT IV VLSI SYSTEM COMPONENTS, CIRCUITS AND SYSTEM LEVEL PHYSICAL DESIGN 09

Multiplexers, Decoders, comparators, priority encoders, Shift registers Arithmetic circuits – Ripple carry adders, Carry look-ahead adders, High-speed adders, Multipliers. Physical design – Delay modelling, cross talk, floor planning, power distribution. Clock distribution.

UNIT V TEST AND TESTABILITY 09

Need for testing, System Partitioning, Layout and testability, Reset/ Initialization, design for testability, testing combinational logic, sequential logic, practical design for test guidelines, scan design techniques, built-in self test.

TOTAL: 45

REFERENCES

1. *Neil H.E. Weste and Kamran Eshraghian, **"Principles of CMOS VLSI Design",** Pearson Education ASIA, 2nd edition, 2000.*
2. *Douglas A. Pucknell, Kamran Eshraghain **"Basic VLSI Design",** Third Edition, Prentice Hall of India Publication, 2010.*
3. *John P.Uyemura ,**"Introduction to VLSI Circuits and Systems",** John Wiley & Sons, Inc., 2002.*
4. *Mark Zwolinski **"Digital system Design with VHDL"** , Second Edition, Pearson Education Pvt .Ltd, New Delhi-2004.*
5. *Eugene D.Fabricius, **"Introduction to VLSI Design",** McGraw Hill International Editions, 1990.*

P13AET103 ADVANCED SIGNAL PROCESSING

L	T	P	C
3	1	0	4

[Review of discrete-time signals and systems- DFT and FFT, Z-Transform, Digital Filters]

UNIT I DISCRETE RANDOM SIGNAL PROCESSING 09

Discrete Random Processes- Ensemble averages, stationary processes, Autocorrelation and Auto covariance matrices- Parameter estimation: Bias and consistency - Parseval's Theorem, White Noise, Power spectrum, Wiener-Khintchine Relation, Filtering random Processes, Spectral Factorization

UNIT II SPECTRUM ESTIMATION

Non-Parametric Methods - Periodogram Estimator, Performance Analysis of Estimators - Unbiased, Consistent Estimators- Modified Periodogram, Bartlett and Welch methods, Blackman –Tukey method. AR, MA, ARMA processes - Yule-Walker equations - Parametric methods of Spectral Estimation

UNIT III LINEAR ESTIMATION AND PREDICTION 09

Linear prediction- Forward and backward predictions, Lattice filter realization, Prony's all pole modeling, Solutions of the Normal equations- Levinson-Durbin recursion - Levinson recursion. Optimum filters- FIR Wiener filter –Causal and Non-causal IIR Wiener filter-Discrete Kalman filter

UNIT IV ADAPTIVE FILTERS 09

FIR adaptive filters -adaptive filter based on steepest descent method- LMS adaptive algorithm, Normalized LMS. Adaptive channel equalization-Adaptive echo cancellation-Adaptive noise cancellation- Adaptive recursive filters (IIR). RLS adaptive filters-Exponentially weighted RLS-sliding window RLS.

UNIT V MULTIRATE DIGITAL SIGNAL PROCESSING 09

Mathematical description of change of sampling rate - Interpolation and Decimation, Decimation by an integer factor - Interpolation by an integer factor, Sampling rate conversion by a rational factor, Multistage implementation of multirate system, Direct form FIR filter structures, Polyphase filter structures, Subband Coding, Quadrature Mirror Filters – Condition for perfect reconstruction, Applications of Multirate systems

L:45; T:15
TOTAL: 60

REFERENCES

1. *Monson H.Hayes, **"Statistical Digital Signal Processing and Modeling"**, John Wiley and Sons, Inc., Singapore, 2004*
2. *John G. Proakis, Dimitris G.Manolakis, **" Digital Signal Processing Pearson Education",** 2002.*
3. *John G. Proakis et.al., **"Algorithms for Statistical Signal Processing', Pearson Education",** 2002.*
4. *Dimitris G.Manolakis et.al., **"Statistical and adaptive signal Processing",** McGraw Hill, New York, 2000.*

P13AET104 EMBEDDED SYSTEMS

L	T	P	C
3	0	0	3

UNIT I EMBEDDED ARCHITECTURE **09**

Embedded Computers, Characteristics of Embedded Computing Applications, Embedded system design process- Requirements, Specification, Architectural Design, Designing Hardware and Software Components, System Integration, Unified modeling language (UML), Formalism for System Design- Structural Description, Behavioral Description, Design Example: Model Train Controller.

UNIT II EMBEDDED PROCESSOR AND COMPUTING PLATFORM **09**

ARM processor- processor and memory organization, Data operations, Flow of Control, TI C55X Digital Signal processor- Processor and Memory organization, Addressing modes, Data operations, Flow of Control, CPU Bus configuration, ARM Bus, SHARC Bus - Design Example : Alarm Clock.

UNIT III NETWORKS **09**

Distributed Embedded Architecture- Hardware and Software Architectures, Networks for embedded systems- I2C, CAN Bus, SHARC link ports, Ethernet, Myrinet, Internet, Network-Based design- Communication Analysis, system performance Analysis, Hardware platform design, Allocation and scheduling, Design Examples: Elevator Controller, Ink jet printer-Hardware Design and Software Design, Personal Digital Assistants, Set-top Boxes.

UNIT IV REAL-TIME CHARACTERISTICS **09**

Clock driven Approach, weighted round robin Approach, Priority driven Approach, Dynamic Versus Static systems, effective release times and deadlines, Optimality of the Earliest deadline first (EDF) algorithm, challenges in validating timing constraints in priority driven systems, Off-line Versus On-line scheduling.

UNIT V REAL TIME OPERATING SYSTEM **09**

Operating system services-Process Management-Memory Management-Device and File Management- I/O sub systems- Interrupt routines in RTOS environment- RTOS –Services-Design using RTOS-Principles-Saving of memory and power, Functions and types of RTOS - RTOS μcos-II

TOTAL: 45

REFERENCES

1. *Wayne Wolf, Computers as Components:* ***"Principles of Embedded Computing System Design",*** *Morgan Kaufman Publishers, 2001.*
2. *Rajkamal,* ***"Embedded System Architecture – Programming and Design"*** *Tata McGraw-Hill, Fifth reprint, 2010*
3. *Jane.W.S. Liu ,* ***"Real-Time systems",*** *Pearson Education Asia, 2000.*
4. *C. M. Krishna and K. G. Shin,* ***"Real-Time Systems",*** *McGraw-Hill, 1997.*
5. *Frank Vahid and Tony Givargi Embedded System Design:* ***"A Unified Hardware/Software Introduction",*** *John Wiley & Sons, 2000.*

P13AEP101 EMBEDDED SYSTEMS LABORATORY

L	T	P	C
0	0	3	1

Experiments based on front-end and back-end tools of the following circuits:

Experiments on ARM Processor

1. Data Operations:
    - Arithmetic Operations
    - Block Transfers
2. I/O Interface
    - LCD Display
    - Matrix Keyboard
    - A/D Conversion
    - D/A conversion
3. Timer Operation – Real Time Clock

Experiments on TMS320C54X using CCS

1. Advanced Addressing Modes
2. Convolution/Correlation of Signals
3. Computation of FFT
4. Audio Capture and Processing
5. Implementation of LMS Algorithm

TOTAL: 45

P13AET201 ANALOG INTEGRATED CIRCUIT DESIGN

L	T	P	C
3	1	0	4

UNIT I BIASING CIRCUITS **09**

Basic current mirrors, cascode current mirrors, active current mirrors, voltage references, supply independent biasing, temperature independent references, PTAT current generation, Constant-Gm Biasing.

UNIT II SINGLE STAGE AMPLIFIERS **09**

Common source stage, Source follower, Common gate stage, Cascode stage, Single ended and differential operation, Basic differential pair, Differential pair with MOS loads

UNIT III FREQUENCY RESPONSE AND NOISE ANALYSIS **09**

Miller effect, Association of poles with nodes, frequency response of common source stage, Source followers, Common gate stage, Cascode stage, Differential pair, Statistical characteristics of noise, noise in single stage amplifiers, noise in differential amplifiers.

UNIT IV OPERATIONAL AMPLIFIERS **09**

Concept of negative feedback, Effect of loading in feedback networks, operational amplifier performance parameters, One-stage Op Amps, Two-stage Op Amps, Input range limitations, Gain boosting, slew rate, power supply rejection, noise in Op Amps.

UNIT V STABILITY AND FREQUENCY COMPENSATION **09**

General considerations, Multipole systems, Phase Margin, Frequency Compensation, Compensation of two stage Op Amps, Slewing in two stage Op Amps, other compensation techniques.

L:45; T:15
TOTAL: 60

REFERENCES

1. *Behzad Razavi,* ***"Design of Analog CMOS Integrated Circuits",*** *Tata McGraw Hill, 2001*
2. *Grebene,* ***"Bipolar and MOS Analog Integrated circuit design",*** *John Wiley & sons,Inc., 2003.*
3. *Kenneth R. Laker, Willy M.C. Sansen, "****Design of Analog Integrated circuits and Systems"****, 1994.*
4. *Phillip E.Allen, DouglasR.Holberg,* ***"CMOS Analog Circuit Design",*** *Second edition, Oxford University Press, 2002*

P13AET202 ADVANCED CONTROL ENGINEERING

L	T	P	C
3	0	0	3

UNIT I INTRODUCTION TO DISCRETE TIME SYSTEMS 09

Introduction discrete systems, Transform methods, properties of Z transform, Solution of difference equation, Inverse Z transform, Simulation Diagram and Signal flow Graphs, Sampled Data control systems, Ideal Sampler, Evaluation of E*(S),Results from the Fourier Transform, Properties of E*(S), Data Reconstruction, Digital to Analog Conversion, Analog to Digital Conversion.

UNIT II STATE SPACE ANALYSIS 09

State space representation of discrete time system, solving discrete time space equation, Pulse transfer function matrix, Continuous time state space equation, Discretization of continuous time state space equation, controllability, observability, useful transformation in state space analysis and design.

UNIT III DESIGN OF DT CONTROL SYSTEM VIA TRANSFORM METHODS 09

Introduction, Obtaining discrete time equivalent of continuous time filter, Discretizing a simple continuous time filter, Backward difference method, Bilinear transformation method, Bilinear transformation method with frequency and prewarping, Impulse invariance method, Step invariance method, matched pole –Zero mapping method, Design principle based on a discrete time equivalent of an analog controller.

UNIT IV TIME RESPONSE AND STABILITY ANALYSIS OF DT SYSTEM 09

Transient analysis and steady state response analysis, transient response specification for second order continuous time system, relationship between Z plane pole and zero location and transient response, steady state error analysis based on root locus method& frequency response method , Bode Diagrams., Stability- Bilinear transformation , Routht Hurwitz criterian, Juris's stability test.

UNIT V DIGITAL CONTROLLER DESIGN 09

Control system specification, Compensation, Phase lag compensation, Phase lead compensation, Design procedure using Bode plot, Integration and Differentiation, Digital PID controllers.

TOTAL: 45

REFERENCES

1. *Katsuhiko Ogata, **"Discrete Time Control System",** Prentice Hall.inc, 1987.*
2. *Charles .L Phillips and H.Troy Nagle, **"Digital control system analysis and design"** Third Edition ,Prentice Hall International Edition.*
3. *M.Gopal **"Digital control and state variable methods**",Tata McGraw publication company limited.*
4. *Norman S. Nise, **"Control Systems Engineering",** John Wiley & Sons, 2008.*

P13AET203 ASIC DESIGN

L	T	P	C
3	0	0	3

UNIT I INTRODUCTION TO ASIC AND LIBRARY DESIGN **09**

Types of ASICs - Design flow – Case Study: SPARC Station 1 – Economies of ASICs – ASIC Cell Libraries – CMOS Transistors - Combinational Logic Cell – Sequential logic cell - Data path logic cell – I/O Cells – Transistor Resistance and Parasitic Capacitance - Logical effort – Library cell design - Library architecture.

UNIT II PROGRAMMABLE ASIC **09**

Anti fuse -Static RAM - EPROM and EEPROM technology – Practical issues - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX – Xilinx Spartan – Virtex FPGAs – Altera Cyclone FPGAs

UNIT III PROGRAMMABLE ASIC I/O **09**

DC inputs and Outputs – Totem Pole output –AC inputs and Outputs – Clock input – Power input – Supply bounce – Noise Margin – Meta-stability - Case Study: Xilinx XC4000 IOB

UNIT IV PROGRAMMABLE ASIC INTERCONNECT **09**

Actel ACT 1/2/3 - Xilinx LCA - Xilinx EPLD - Altera MAX 5000/7000/9000 - Altera FLEX FPGAs – Case study: Spartan-3 Block RAM

UNIT V LOGIC SIMULATION & SYNTHESIS **09**

Types of simulation – Logic systems – How logic Simulation works – Delay models – Limitations of Logic simulation – Static Timing analysis - Design Systems - Logic synthesis – EDIF – Schematic Entry – Inside a logic Synthesizer – Case Study: Comparator/MUX

TOTAL: 45

REFERENCES

1. *M.J.S .Smith, **"Application Specific Integrated Circuits"**, Addison -Wesley Longman Inc., 1997.*
2. *Wayne Wolf, **"FPGA-Based System Design"**, Prentice Hall PTR, 2004.*
3. *R. Rajsuman and Santa Clara, **"System-on-a-Chip Design and Test"**, CA: Artech House Publishers, 2000.*
4. *F. Nekoogar, **"Timing Verification of Application-Specific Integrated Circuits (ASICs)"**, Prentice Hall PTR, 1999.*

P13AEP201 VLSI LABORATORY

L	T	P	C
0	0	3	1

Experiments based on front-end and back-end tools of the following circuits:

Using Xilinx ISE front-end software (VHDL only)

Combinational logic:

1. 4-bit parallel adder
2. 4-bit serial adder
3. Parallel multipliers
4. Multiply Accumulate unit

Sequential logic:

1. Multi-bit pre-settable, up/down counters
2. FIFO buffer
3. Sequence detectors
4. Real-time Clock

Using Microwind /Cadence back-end software:

1. 4-bit parallel adder
2. 4-bit serial adder
3. 4-bit pre-settable, up/down counters
4. 16 byte FIFO buffer
5. 3-bit Sequence detectors

TOTAL: 45

P13AETE01 ADVANCED DIGITAL IMAGE PROCESSING

L	T	P	C
3	0	0	3

UNIT I IMAGE REPRESENTATION AND COLOR IMAGE PROCESSSING 09

Image acquisition- Psycho-visual model for monochrome image- Image digitization- Color Fundamentals-Color Models-The RGB, CMY, CMYK and HSI Color Model- Pseudo color Image Processing - Intensity Slicing- Gray to Color transformations -Basics of Color Image Processing-Color Image Smoothing and Sharpening- Color Segmentation - Noise in Color Images.

UNIT II SEGMENTATION AND TEXTURE ANALYSIS 09

Edge Linking and Boundary Detection - Local Processing-Global Processing –Thresholding-Segmentation by Morphological Watershed Segmentation Algorithm - Use of Markers- Use of Motion in Segmentation-Spatial Techniques-Frequency Domain Techniques-Texture- Statistical, Syntactic and Hybrid texture description - texture recognition and applications.

UNIT III OBJECT RECOGNITION 09

Patterns and Pattern Classes -Recognition Based on Decision-Theoretic Methods -Matching - Optimum Statistical Classifiers- Neural Networks, Structural Methods -Matching Shape Numbers-String Matching-Syntactic Recognition of Strings-Syntactic Recognition of Trees - Fuzzy Systems - GA.

UNIT IV MORPHOLOGICAL IMAGE PROCESSING 09

Preliminaries- Some Basic Concepts from Set Theory-Logic Operations Involving Binary Images -Dilation and Erosion -Hit-or-Miss Transformation - Basic Morphological Algorithms -Boundary Extraction- Region Filling- Extraction of Connected Components- Convex Hull- Thinning-Thickening- Skeletons- Pruning- Summary of Morphological Operations on Binary Images-Extensions to Gray-Scale Images- - Applications of Gray-Scale Morphology

UNIT V IMAGE PROCESSING APPLICATIONS 09

Image compression- JPEG, JPEG2000 and MPEG standards- Watermarking-Steganography-3D vision tasks- Marr's theory, active and purposive vision- Geometry for 3D vision-Use of 3D vision-Shape from X-shape - motion, texture- Full 3D objects.

TOTAL: 45

REFERENCES

1. *Rafael C. Gonzalez,* ***"Digital Image Processing",*** *Pearson Education, Inc., II Edition, 2002*
2. *Milman Sonka, Vaclav Hlavac, Roger Boyle,* ***"Image Processing, Analysis and Machine Vision",*** *Brooks/Cloe, Vikas Publishing House 2nd Edition, 1999.*
3. *David Salomon,* ***"Data Compression-The Complete Reference",*** *Springer Verlag New York Inc., 2nd Edition, 2001*
4. *Rafael C. Gonzalez, Richards E.Woods, Steven Eddins, "****Digital Image Processing using MATLAB"****, Pearson Education, Inc., 2004.*
5. *Willam K.Pratt,* ***"Digital Image Processing",*** *John Wiley, New York, 2002.*

P13AETE02 NEURAL NETWORKS AND APPLICATIONS

L	T	P	C
3	0	0	3

UNIT I INTRODUCTION TO ARTIFICIAL NEURAL NETWORKS 09

Neuro-physiology - General Processing Element - ADALINE - LMS learning rule - MADALINE - MR2 training algorithm.

UNIT II BPN AND BAM 09

Back Propagation Network - updating of output and hidden layer weights -application of BPN – associative memory - Bi-directional Associative Memory - Hopfield memory - traveling sales man problem.

UNIT III SIMULATED ANNEALING AND CPN 09

Annealing, Boltzmann machine - learning - application - Counter Propagation network - architecture -training - Applications.

UNIT IV SOM AND ART 09

Self organizing map - learning algorithm - feature map classifier - applications - architecture of Adaptive Resonance Theory - pattern matching in ART network.

UNIT V NEOCOGNITRON 09

Architecture of Neocognitron - Data processing and performance of architecture of spacio - temporal networks for speech recognition.

TOTAL: 45

REFERENCES

1. *J.A. Freeman and B.M.Skapura , "**Neural Networks, Algorithms Applications and Programming Techniques",** Addison-Wesely,2003.*
2. *Laurene Fausett, "**Fundamentals of Neural Networks: Architecture, Algorithms and Applications",** Prentice Hall, 1994.*
3. *Simon Haykin, **"Neural Networks & Learning Machines"** third edition Pearson Education 2011.*
4. *Martin T. Hagan, Howard B. Demuth, Mark Beale, **" Neural Network Design ",** Thomson and Learning, Third Reprint 2003.*

P13AETE03 LOW POWER VLSI DESIGN

L	T	P	C
3	0	0	3

UNIT I POWER DISSIPATION IN CMOS **09**

Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS devices- Basic principle of low power design.

UNIT II POWER ESTIMATION **09**

Power estimation techniques – Logic level power estimation – Simulation power analysis– Probabilistic power analysis.

UNIT III POWER OPTIMIZATION **09**

Logical level power optimization – Circuit level low power design – Circuit techniques for reducing power consumption in adders and multipliers.

UNIT IV DESIGN OF LOW POWER CMOS CIRCUITS **09**

Computer Arithmetic techniques for low power systems – Reducing power consumption in memories – Low power clock, Interconnect and layout design – Advanced techniques – Special techniques.

UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER **09**

Synthesis for low power – Software of low power- Software for Power optimization Behavioral level transforms- Software design for low power – co-design for low power. Case study: sub 28 nanometer chip design

TOTAL: 45

REFERENCES

1. *K.Roy and S.C. Prasad , **"Low Power CMOS VLSI circuit design",** Wiley,2000*
2. *Gary Yeap, **"Practical low power digital VLSI design",** Kluwer, 2001.*
3. *Dimitrios Soudris, Chirstian Pignet, Costas Goutis, **"Designing CMOS Circuits For Low Power",** Kluwer,2002*
4. *J.B. Kuo and J.H Lou, **"Low voltage CMOS VLSI Circuits",** Wiley 1999.*
5. *A.P.Chandrakasan and R.W. Broadersen, **"Low power digital CMOS design",** Kluwer, 1995.*
6. *Abdellatif Bellaouar, Mohamed.I. Elmasry, **"Low power digital VLSI Design",** Kluwer, 1995.*
7. *James B. Kuo, Shin – chia Lin, **"Low voltage SOI CMOS VLSI Devices and Circuits",** John Wiley and sons, inc 2001*

P13AETE04 DSP INTEGRATED CIRCUITS

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UNIT I NUMBER SYSTEMS, ARITHMETIC UNITS AND INTEGRATED CIRCUIT DESIGN **09**

Conventional number system, Redundant Number system, Residue Number System .Bit-parallel and Bit-Serial arithmetic, Distributed Arithmetic, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-Accumulator.

UNIT II DIGITAL SIGNAL PROCESSING **09**

Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal-processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, FFT-The Fast Fourier Transform Algorithm, Image coding, Discrete cosine transforms.

UNIT III DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS **09**

FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects -Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

UNIT IV DSP INTEGRATED CIRCUITS AND VLSI CIRCUIT TECHNOLOGIES **09**

Standard digital signal processors, Application specific IC's for DSP, DSP systems, DSP system design, Integrated circuit design. MOS transistors, MOS logic, VLSI process technologies, Trends in CMOS technologies.

UNIT V DSP ARCHITECTURES AND SYNTHESIS **09**

DSP system architectures, Standard and Ideal DSP architecture, Multiprocessors and multi computers, Systolic and Wave front arrays, Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs, Layout of VLSI circuits, FFT processor, DCT processor and Interpolator as case studies.

TOTAL: 45

REFERENCES

1. *Lars Wanhammer,* ***"DSP Integrated Circuits",*** *Academic press, New York 1999.*
2. *A.V.Oppenheim et.al,* ***"Discrete-time Signal Processing",*** *Pearson education, 2000.*
3. *Emmanuel C. Ifeachor, Barrie W. Jervis,* ***"Digital signal processing – A practical approach",*** *2nd edition, Prentice Hall, 2001.*
4. *Keshab K.Parhi,* ***'VLSI digital Signal Processing Systems design and Implementation",*** *John Wiley & Sons, 1999.*

P13AETE05 ADVANCED COMPUTER ARCHITECTURE

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UNIT I PRINCIPLES OF PARALLEL PROCESSING 09

Multiprocessors and Multicomputers – Multivector and SIMD Computers- PRAM and VLSI Models- Conditions of Parallelism- Program Partitioning and scheduling-program flow mechanisms- speed up performance law.

UNIT II PROCESSOR AND MEMORY ORGANIZATION 09

Advanced processor technology – Superscalar and vector processors- Memory hierarchy technology- Virtual memory technology- Eleven advanced optimization of cache performance.

UNIT III PIPELINE AND PARALLEL ARCHITECTURE 09

Linear pipeline processors- Non linear pipeline processors- Instruction pipeline design- Arithmetic design- Superscalar and super pipeline design-Message passing mechanisms

UNIT IV VECTOR, MULTITHREAD AND DATAFLOW ARCHITECTURE 09

Vector processing principle- Compound Vector processing-Principles of multithreading- scalable and multithread architectures – Dataflow and hybrid architectures.

UNIT V SOFTWARE AND PARALLEL PROGRAMMING 09

Parallel programming models – Parallel Languages and compilers - parallel programming environments- message passing program development- multiprocessor UNIX design goals- MACH/OS kernel architecture- OSF/1 architecture and applications.

TOTAL: 45

REFERENCES

1. *Kai Hwang, **"Advanced Computer Architecture",** Tata McGraw Hill 2009*
2. *John L. Hennessey and David A. Patterson**," Computer Architecture: A Quantitative Approach",** Fourth Edition, Morgan Kaufmann, 2007.William Stallings, "Computer Organization and Architecture", McMillan Publishing Company, 1990.*
3. *William Stallings, **" Computer Organization and Architecture",** MacMillan Publishing Company, 1990*
4. *H.S. Stone, **"High-performance Computer Architecture",** 3rd edition, Addison-Wesley, 1993.*

P13AETE06 HARDWARE SOFTWARE CO-DESIGN

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UNIT I SYSTEM SPECIFICATION AND MODELLING 09

Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification and Modelling, Co-Design for Heterogeneous Implementation – Processor Synthesis, Single-Processor Architectures with one ASIC, Single-Processor Architectures with many ASICs, Multi-Processor Architectures Comparison of Co-Design Approaches, Models of Computation, Requirements for Embedded System Specification .

UNIT II HARDWARE/SOFTWARE PARTITIONING 09

Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms.

UNIT III HARDWARE/SOFTWARE CO-SYNTHESIS 09

Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis.

UNIT IV PROTOTYPING AND EMULATION 09

Introduction, Prototyping and Emulation Techniques, Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping, Target Architecture- Architecture Specialization Techniques, System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems, Mixed Systems and Less Specialized Systems

UNIT V DESIGN SPECIFICATION AND VERIFICATION 09

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification, Languages for System Level Specification and Design System - Level Specification, Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co-simulation

TOTAL: 45

REFERENCES

1. *Ralf Niemann , **"Hardware/Software Co-Design for Data Flow Dominated Embedded Systems"**, Kluwer Academic Pub, 1998*
2. *Jorgen Staunstrup , Wayne Wolf , **"Hardware/Software Co-Design: Principles and Practice"** , Kluwer Academic Pub,1997.*
3. *Giovanni De Micheli , Rolf Ernst Morgon, **"Reading in Hardware/Software Co-Design"** Kaufmann Publishers,2001*
4. *Patrick Schaumont, "**A Practical Introduction to Hardware/Software Codesign", Springer,** 2009*

P13AETE07 DESIGN AND ANALYSIS OF ALGORITHMS

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UNIT I INTRODUCTION **09**

Polynomial and Exponential algorithms, big "o" and small "o" notation, exact algorithms and heuristics, direct / indirect / deterministic algorithms, static and dynamic complexity, stepwise refinement.

UNIT II DESIGN TECHNIQUES **09**

Subgoals method, working backwards, work tracking, branch and bound algorithms for traveling salesman problem and knapsack problem, hill climbing techniques, divide and conquer method, dynamic programming, greedy methods.

UNIT III SEARCHING AND SORTING **09**

Sequential search, binary search, block search, Fibonacci search, bubble sort, bucket sorting, quick sort, heap sort, average case and worst case behavior, FFT.

UNIT IV GRAPH ALGORITHMS **09**

Minimum spanning, tree, shortest path algorithms, R-connected graphs, Even's and Kleitman's algorithms, ax-flow min cut theorem, Steiglitz's link deficit algorithm.

UNIT V SPECIAL ALGORITHMS **09**

NP Completeness Approximation Algorithms, NP Hard Problems, Strasseu's Matrix Multiplication Algorithms, Magic Squares, Introduction To Parallel Algorithms and Genetic Algorithms, Monti-Carlo Methods, Amortised Analysis.

TOTAL: 45

REFERENCES

1. *Sara Baase, "**Computer Algorithms: Introduction to Design and Analysis**", Addison Wesley, 1988.*
2. *T.H.Cormen, C.E.Leiserson and R.L.Rivest, "**Introduction to Algorithms",** Mc Graw Hill, 1994.*
3. *E.Horowitz and S.Sahni, "**Fundamentals of Computer Algorithms**", Galgotia Publications, 1988.*
4 *D.E.Goldberg, "**Genetic Algorithms: Search Optimization and Machine Learning**", Addison Wesley, 1989.*

P13AETE08 SOFT COMPUTING

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UNIT I ARTIFICIAL NEURAL NETWORKS **09**

Supervised learning Neural networks-Introduction, Perception- Adaline, Back propagation- Multi layer perception- Unsupervised learning and other Neural networks-Introduction, Competitive learning networks, Kohenen self organizing networks, Learning vector quantization, Hebbian learning, Hopfield network , Content addressable nature, Binary Hopfield network, Continuous-valued Hopfield network , Travelling Salesperson problem.

UNIT II FUZZY SET THEORY **09**

Fuzzy sets, Basic definitions and terminology, Member function formulation & parameterization, Fuzzy rules , fuzzy reasoning - Extension principle, Fuzzy relation, Fuzzy inference systems: Mamdani model, Sugeno model. Tsukamoto model, Input space partitioning, Fuzzy modeling.

UNIT III OPTIMIZATION **09**

Derivative based optimization-Descent methods, Method of steepest descent, Classical Newtons method, Step-size determination; Derivative free optimization- Genetic algorithm, Simulated annealing, Random search, Downhill search.

UNIT IV ADVANCED NEURO-FUZZY MODELLING **09**

Classification and regression trees, decision tress, Cart algorithm – Data clustering algorithms: K- means clustering, Fuzzy C-means clustering, Mountain clustering, Subtractive clustering – rule base structure, Input space partitioning, rule based organization, focus set based rule combination; Neuro-fuzzy control: Feedback Control Systems, Expert Control, Inverse Learning, Specialized Learning, Back propagation through real time Recurrent Learning.

UNIT V GENETIC ALGORITHM **09**

Fundamentals of genetic algorithm- Basic concepts - Encoding – Binary, Octal, Hex, Permutation, Value and tree, Reproduction- Roulette-wheel selection, Boltzman selection, Tournament selection, Rank selection, Steady state selection, Crossover single site, Two point, Multi point, Uniform and matrix, Crossover rate, Inversion, Deletion and duplication, Deletion and Regeneration, Segregation, Crossover, Mutation, Generational cycle.

TOTAL: 45

REFERENCES

1. *Jang J.S.R.,Sun C.T and Mizutani E,* ***"Neuro Fuzzy and Soft computing",*** *Pearson education (Singapore) 2004.*
2. *S.Rajasekaran and G.A.Vijayalakshmi Pai,* ***"Neural networks,Fuzzy logics,and Genetic algorithms",*** *Prentice Hall of India,2003.*
3. *David E.Goldberg,* ***"Genetic Algorithms in Search, Optimization, and Machine Learning",*** *Pearson Education, Asia,1996*
4. *Laurene Fauseett,* ***"Fundamentals of Neural Networks",*** *Prentice Hall India, New Delhi,1994.*
5. *Timothy J.Ross,* ***"Fuzzy Logic Engineering Applications",*** *McGrawHill,NewYork,1997.*

P13COTE09 INTERNETWORKING MULTIMEDIA

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UNIT I INTRODUCTION TO MULTIMEDIA **09**

Digital sound, video and graphics, basic multimedia networking, multimedia characteristics, evolution of Internet services model, network requirements for audio/ video transform, multimedia coding and compression for text, image, audio and video.

UNIT II SUBNETWORK TECHNOLOGY **09**

Broadband services, ATM and IP, IPV6, High speed switching, resource reservation, Buffer management, traffic shaping, caching, scheduling, and policing, throughput, delay and jitter performance.

UNIT III MULTIMEDIA NETWORKING APPLICATIONS **09**

MIME, Peer- to-Peer computing, shared application, video conferencing, centralized and distributed conference control, distributed virtual reality, light weight session philosophy.

UNIT IV MULTIMEDIA COMMUNICATION STANDARDS **09**

Objective of MPEG- 7 standard, Functionalities and systems of MPEG-7, MPEG-21 Multimedia Framework Architecture, - Content representation, Content Management and usage, Intellectual property management, Audio visual system- H322: Guaranteed QOS LAN systems; MPEG_4 video Transport across internet.

UNIT V MULTIMEDIA COMMUNICATION ACROSS NETWORKS **09**

Packet Audio/video in the network environment, video transport across Generic networks- Layered video coding, error Resilient video coding techniques, Scalable Rate control, Streaming video across Internet, Multimedia transport across ATM networks and IP network, Multimedia across wireless networks.

TOTAL: 45

REFERENCES

1. *Jon Crowcroft, Mark Handley, Ian Wakeman,* ***"Internetworking Multimedia",*** *Harcourt Asia Pvt. Ltd. Singapore, 1998.*
2. *B.O. Szuprowicz,* ***"Multimedia Networking",*** *McGraw Hill, Newyork, 1995.*
3. *Tay Vaughan,* ***"Multimedia - Making it to work",*** *4ed, Tata McGraw Hill, NewDelhi, 2000.*
4. *K.R.Rao, Zoran S. Bojkovic and Dragorad A. Milovanovic,* ***"Multimedia Communication Systems"****, PHI , 2003.*

P13AETE09 DSP PROCESSOR ARCHITECTURE AND PROGRAMMING

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UNIT I FUNDAMENTALS OF PROGRAMMABLE DSPs **09**

Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in P-DSPs – Multiple access memory – Multi-port memory –VLIW architecture- Pipelining –Special Addressing modes in P-DSPs – On-chip Peripherals.

UNIT II TMS320C5X PROCESSOR **09**

Architecture – Assembly language syntax - Addressing modes – Assembly language Instructions - Pipeline structure, Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals.

UNIT III TMS320C3X PROCESSOR **09**

Architecture – Data formats - Addressing modes – Groups of addressing modes- Instruction sets - Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals – Generating and finding the sum of series, Convolution of two sequences, Filter design – Introduction to code composer studio

UNIT IV ADSP PROCESSORS **09**

Architecture of ADSP-21XX and ADSP-210XX series of DSP processors- Addressing modes and assembly language instructions – Application programs –Filter design, FFT calculation.

UNIT V ADVANCED DSP PROCESSORS **09**

Architecture of TMS320C54X: Pipe line operation, Code Composer studio - Architecture of TMS320C6X - Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors**.**

TOTAL: 45

REFERENCES

1. *B.Venkataramani and M.Bhaskar,* ***"Digital Signal Processors – Architecture, Programming and Applications",*** *Tata McGraw – Hill Publishing Company Limited, New Delhi, 2003.*
2. ***"User guides"****- Texas Instruments, Analog Devices, Motorola.*
3. *Lapsley et al,* ***"DSP Processor Fundamentals, Architectures & Features"****, S. Chand & Co, 2000.*

P13COTE11 HIGH PERFORMANCE COMMUNICATION NETWORKS

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UNIT I PACKET SWITCHED NETWORKS **09**

OSI and IP models, Ethernet (IEEE 802.3), Token ring (IEEE 802.5), Wireless LAN (IEEE 802.11) FDDI, DQDB, SMDS: Internetworking with SMDS.

UNIT II ISDN **09**

ISDN - overview, interfaces and functions, ISDN Layers – Physical, Data link and Network layers ISDN services - Signaling System 7 (SS7).

UNIT III BROADBAND ISDN AND ATM **09**

BISDN: Broadband ISDN standards, services, architecture and Protocol reference model. ATM: Main features-addressing, signaling and routing, ATM header structure- Adaptation Layer, management and control.

UNIT IV ADVANCED NETWORK ARCHITECTURE **09**

IP forwarding architectures overlay model, Multi Protocol Label Switching (MPLS), integrated services in the Internet, Resource Reservation Protocol (RSVP), Differentiated services.

UNIT V BLUE TOOTH TECHNOLOGY **09**

The Blue tooth module-Protocol stack Part I: Antennas, Simple RF architecture, The Link controller operation, Piconet and scatternet operation, Baseband/Link controller Architectural overview; The Blue tooth module-Protocol stack Part II: Logical link control and adaptation protocol – L2CAP signalling, Service discovery protocol, Wireless access protocol, Telephony control protocol

TOTAL: 45

REFERENCES

1. *Jean Walrand and Pravin Varaiya , **"High Performance Communication networks",** 2nd edition, Harcourt and Morgan Kauffman, London, 2000.*
2. *William Stallings, **"ISDN and Broadband ISDN with Frame Relay and ATM",** 4th edition, Pearson education Asia, 2002.*
3. *Lenon gracia Widjaya, **"Communication Network",** Tata McGraw Hill, New Delhi 2000*
4. *Ranier Handel Manfred N Huber, Stefan Schrodder, **"ATM Networks - Concepts, Protocols Applications"**, 3rd Edition Addison Wesley, New York, 1999.*

P13COTE12 HIGH SPEED SWITCHING ARCHITECTURE

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UNIT I HIGH SPEED NETWORK **09**

Introduction- LAN, WAN, Network evolution through ISDN to B-ISDN, Transfer mode and control of B-ISDN, SDH multiplexing structure, ATM standard, ATM adaptation layers.

UNIT II LAN SWITCHING TECHNOLOGY **09**

Switching Concepts, switch forwarding techniques, switch path control, LAN Switching, cut-through forwarding, store and forward, virtual LANs

UNIT III ATM SWITCHING ARCHITECTURE **09**

Switch model, ATM,QOS, Blocking networks - basic - and- enhanced banyan networks, sorting networks - merge sorting, re-arrangable networks - full-and- partial connection networks, non blocking networks - Recursive network construction, comparison of non-blocking network, Switching with deflection routing - shuffle switch, tandem banyan

UNIT IV QUEUES IN ATM SWITCHES **09**

Internal Queuing -Input, output and shared queuing, multiple queuing networks – Combined Input, output and shared queuing - performance analysis of Queued switches.

UNIT V IP SWITCHING **09**

Addressing model, IP Switching types - flow driven and topology driven solutions, IP Over ATM address and next hop resolution, multicasting, Photonic switching - Photonic switching architectures.

TOTAL: 45

REFERENCES

1. *Achille Pattavina,* ***"Switching Theory: Architectures and performance in Broadband ATM networks ",*** *John Wiley & Sons Ltd, New York. 1998.*
2. *Christopher Y Metz,* ***"Switching protocols & Architectures",*** *McGraw – Hill Professional Publishing, NewYork.1998.*
3. *Rainer Handel, Manfred N Huber, Stefan Schroder,* ***"ATM Networks – Concepts Protocols, Applications",*** *III Edition, Addison Wesley, New York. 1999.*
4. *John A.Chiong,* ***"Internetworking ATM for the internet and enterprise networks",*** *McGraw Hill, New York, 1998.*
5. *S.Kar and T.Srinivas,* ***"Optical fiber communications, Principles and Practice",*** *Tata McGraw Hill, 2002.*

P13AETE10 VLSI SIGNAL PROCESSING

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UNIT I INTRODUCTION TO DSP SYSTEMS **09**

Introduction To DSP Systems -Typical DSP algorithms; Iteration Bound – data flow graph representations, loop bound and iteration bound, Longest path Matrix algorithm; Pipelining and parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.

UNIT II RETIMING **09**

Retiming - definitions and properties; Unfolding – an algorithm for Unfolding, properties of unfolding, sample period reduction and parallel processing application; Algorithmic strength reduction in filters and transforms – 2-parallel and Fast FIR filter, DCT algorithm - architecture, parallel architectures for rank-order filters.

UNIT III FAST CONVOLUTION **09**

Fast convolution – Cook-Toom & Modified Cook-Took algorithm; Pipelined and parallel recursive and adaptive filters – inefficient/efficient single channel interleaving, Look- ahead pipelining in first- order IIR filters, Look-ahead pipelining with power-of-two decomposition, Clustered Look-ahead pipelining, parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters, pipelined adaptive digital filters, relaxed look-ahead, pipelined LMS adaptive filter.

UNIT IV BIT-LEVEL ARITHMETIC ARCHITECTURES **09**

Scaling and roundoff noise, state variable description of digital filters, scaling and roundoff noise computation, roundoff noise in pipelined first-order filters; Bit-Level Arithmetic Architectures-parallel multipliers with sign extension, carry-ripple array multipliers, carry-save multiplier, 4x4 Baugh-Wooley carry-save multiplication tabular form and implementation, design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, multiplication using Horner's rule for precision improvement.

UNIT V PROGRAMMING DIGITAL SIGNAL PROCESSORS **09**

Numerical Strength Reduction – sub-expression elimination, multiple constant multiplications, iterative matching - Linear transformations -Synchronous, Wave and asynchronous pipelining-clocking styles, clock skew in edge-triggered single-phase clocking, two-phase clocking, wave pipelining, asynchronous pipelining bundled data vs dual rail protocol - Digital Signal Processors –general architecture -features -Low Power Design – need, charging and discharging capacitance, short-circuit current of inverter, CMOS leakage current, principles of low power design.

TOTAL: 45

REFERENCES

1. *Keshab K.Parhi,* ***"VLSI Digital Signal Processing systems, Design and implementation",*** *Wiley Inter Science, 1999.*
2. *Gary Yeap,* ***"Practical Low Power Digital VLSI Design",*** *Kluwer Academic Publishers, 1998.*
3 *Mohammed Isamail and Terri Fiez,* ***"Analog VLSI Signal and Information Processing",*** *McGraw-Hill, 1994*
4 *S.Y. Kung, H.J. White House, T. Kailath,* ***"VLSI and Modern Signal Processing",*** *PHI, 1985.*
5. *Jose E. France, Yannis Tsividis,* ***"Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing"****, Prentice Hall, 1994.*

P13AETE11 ANALOG VLSI DESIGN

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UNIT I BASIC CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW-VOLTAGE SIGNAL PROCESSING **09**

Signal VLSI Chips-Basic CMOS Circuits-Basic Gain Stage-Gain Boosting Techniques- Super MOSTransistor- Primitive Analog Cells-Linear Voltage-Current Converters-MOS Multipliers and Resistors-CMOS,Bipolar and Low-Voltage BiCMOS Op-Amp Design-Instrumentation Amplifier Design-Low Voltage Filters.

UNIT II BASIC BICMOS CIRCUIT TECHNIQUES, CURRENT -MODE SIGNAL AND NEURAL INFORMATION PROCESSING **09**

Continuous-Time Signal Processing-Sampled-Data Signal Processing-Switched-Current Data Converters-Practical Considerations in SI Circuits Biologically-Inspired Neural Networks - Floating - Gate, Low-Power Neural Networks-CMOS Technology and Models- Design Methodology-Networks-Contrast Sensitive Silicon Retina.

UNITIII SAMPLED-DATA ANALOG FILTERS, OVER SAMPLED A/D CONVERTERS AND ANALOG INTEGRATED SENSORS **09**

First-order and Second SC Circuits-Bilinear Transformation - Cascade Design-Switched-Capacitor Ladder Filter-Synthesis of Switched-Current Filter- Nyquist rate A/D Converters-Modulators for Over sampled A/D Conversion-First and Second Order and Multibit Sigma-Delta Modulators-Interpolative Modulators –Cascaded Architecture- Decimation Filters-mechanical, Thermal, Humidity and Magnetic Sensors-Sensor Interfaces.

UNIT IV DESIGN FOR TESTABILITY AND ANALOG VLSI INTERCONNECTS **09**

Fault modelling and Simulation - Testability-Analysis Technique-Ad Hoc Methods and General Guidelines-Scan Techniques-Boundary Scan-Built-in Self Test-Analog Test Buses- Design for Electron -Beam Testablity-Physics of Interconnects in VLSI-Scaling of Interconnects-A Model for Estimating Wiring Density-A Configurable Architecture for Prototyping Analog Circuits.

UNIT V STATISTICAL MODELING AND SIMULATION, ANALOG COMPUTER-AIDED DESIGN AND ANALOG AND MIXED ANALOG-DIGITAL LAYOUT **09**

Review of Statistical Concepts - Statistical Device Modeling- Statistical Circuit Simulation-Automation Analog Circuit Design-automatic Analog Layout-CMOS Transistor Layout-Resistor Layout-Capacitor Layout-Analog Cell Layout-Mixed Analog -Digital Layout

TOTAL: 45

REFERENCES

1. *Mohammed Ismail, Terri Fiez, **"Analog VLSI signal and Information Processing ",** McGraw-Hill International Editons, 1994.*
2. *Malcom R.Haskard, Lan C.May, **"Analog VLSI Design - NMOS and CMOS ",** Prentice Hall, 1998.*
3. *Randall L Geiger, Phillip E. Allen, " Noel K.Strader, "**VLSI Design Techniques for Analog and Digital Circuits ",** Mc Graw Hill International Company, 1990.*
4. *Jose E.France, Yannis Tsividis, **"Design of Analog-Digital VLSI Circuits for Telecommunication and signal Processing ",** Prentice Hall, 1994.*

P13AETE12 COMPUTER AIDED DESIGN OF VLSI CIRCUITS

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UNIT I VLSI DESIGN METHODOLOGIES **09**

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.

UNIT II LAYOUT & PARTITIONING **09**

Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms – partitioning

UNIT III FLOORPLANNING & ROUTING **09**

Floor planning concepts - shape functions and floor plan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

UNIT IV SIMULATION & SYNTHESIS **09**

Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT V HIGH LEVEL SYNTHESIS **09**

High level Synthesis - Hardware models - Internal representation - Allocation assignment and scheduling - Simple scheduling algorithm - Assignment problem – High level transformations.

TOTAL: 45

REFERENCES

1. *S.H. Gerez, "**Algorithms for VLSI Design Automation", John Wiley & Sons,2002.*
2. *N.A. Sherwani, "**Algorithms for VLSI Physical Design Automation**", Kluwar Academic Publishers, 2002*
3. *Drechsler, R., **"Evolutionary Algorithms for VLSI CAD", Kluwer Academic Publishers, Boston, 1998.***
4. *Hill, D., D. Shugard, J. Fishburn and K. Keutzer, **"Algorithms and Techniques for VLSI Layout Synthesis", Kluwer Academic Publishers, Boston, 1989.***

P13AETE13 STOCHASTIC MODELS AND SIMULATION

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UNIT I INTRODUCTION TO PROBABILITY **09**

Sample space and events; Probability axiom; Conditional probability; Independent events, Bayes formula, Simple problems.

UNIT II RANDOM VARIABLE & DISTRIBUTIONS **09**

Random Variables, Distribution functions, continuous and discrete random variables, Bernoulli, Binomial, Geometric, Poisson random variables, uniform, exponential, normal random variables, jointly distributed random variables, expectations and moment generating functions, – Properties, simulation samples for the above mentioned distributions.

UNIT III MARKOV CHAINS **09**

Markov chains, Chapman – Kolmogorov equations, Classification of states, examples of Markov chains. Gamblers ruin problem, mean time spent in transient states, Branching process.

UNIT IV POISSON PROCESSES **09**

Properties of exponential distribution, convolution of exponential random variables, Poisson process. Inter arrival of waiting time distribution, Applications to reliability problems, Estimating software reliability.

UNIT V RENEWAL THEORY, QUEUING THEORY & SIMULATION **09**

Renewal Theory - examples, distribution of the counting process N(t), alternating renewal process, Regenerative process, computing the renewal function, semi – Markov process, Computation of renewal function, Poisson process as a renewal process. Single server exponential queuing system, Queue with finite capacity, Shoe shine shop, network of queues, open and closed systems. Methods of simulation of random variables – Inverse transformation method, Rejection method.

TOTAL: 45

REFERENCES

1. *Sheldon M. Ross,* ***"Introduction to Probability Models",*** *Academic press, 2005.*
2. *Karlin and H.M. Tailor,* ***"A First Course in Stochastic Processes",*** *Academic Press, 1975.*
3. *B. L. Nelson ,* ***"Stochastic Modeling: Analysis and Simulation"****. McGraw-Hill, New York 1995.*
4. *Sheldon M.Ross,* ***"A First Course in Probability",*** *Sixth Edition, Prentice Hall, New Jersey, 2002*

P13AETE14 MOBILE COMPUTING

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UNIT I INTRODUCTION **09**

Medium Access Control : Motivation for Specialized MAC- SDMA- FDMA- TDMACDMA- Comparison of Access mechanisms – Tele communications : GSM- DECTTETRA – UMTS- IMT-200 – Satellite Systems: Basics- Routing- Localization- Handover- Broadcast Systems: Overview – Cyclic Repetition of Data- Digital Audio Broadcasting – Digital Video Broadcasting

UNIT II WIRELESS NETWORKS **09**

Wireless LAN: Infrared Vs Radio Transmission – Infrastructure Networks- Ad hoc Networks- IEEE 802.11 – HIPERLAN – Bluetooth- Wireless ATM: Working Group- Services- Reference Model – Functions – Radio Access Layer – Handover- Location Management- Addressing Mobile Quality of Service- Access Point Control Protocol

UNIT III MOBILE NETWORK LAYER **09**

Mobile IP : Goals – Assumptions and Requirement – Entities – IP packet Delivery- Agent Advertisement and Discovery – Registration – Tunneling and Encapsulation – Optimization – Reverse Tunneling – IPv6 – DHCP- Ad hoc Networks

UNIT IV MOBILE TRANSPORT LAYER **09**

Traditional TCP- Indirect TCP- Snooping TCP- Mobile TCP- Fast retransmit/ Fast Recovery- Transmission/ Timeout Freezing – Selective Retransmission- Transaction Oriented TCP

UNIT V WAP **09**

Architecture – Datagram Protocol- Transport Layer Security- Transaction Protocol- Session Protocol- Application Environment-Wireless Telephony Application

TOTAL: 45

REFERENCES

1. *1. J.Schiller, **"Mobile Communication",** Addison Wesley, 2000.*
2. *William Stallings, **"Wireless Communication and Networks",** Pearson Education,2003.*
3 *William C.Y.Lee, **"Mobile Communication Design Fundamentals",** John Wiley,1993.*
4 *Singhal, **"WAP-Wireless Application Protocol",** Pearson Education, 2003*

P13AETE15 CELLULAR AND MOBILE COMMUNICATION

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UNIT I INTRODUCTION TO WIRELESS MOBILE COMMUNICATIONS 09

History and evolution of mobile radio systems. Types of mobile wireless services / systems - Cellular, WLL, Paging, Satellite systems, Standards, Future trends in personal wireless systems.

UNIT II CELLULAR CONCEPT AND SYSTEM DESIGN FUNDAMENTALS 09

Cellular concept and frequency reuse, Multiple Access Schemes, Channel assignment and handoff, Interference and system capacity, Trunking and Erlang capacity calculations.

UNIT III MOBILE RADIO PROPAGATION 09

Radio wave propagation issues in personal wireless systems, Propagation models, Multipath fading and base band impulse response models, Parameters of mobile multipath channels, Antenna systems in mobile radio.

UNIT IV MODULATION AND SIGNAL PROCESSING 09

Analog and digital modulation techniques, Performance of various modulation techniques – Spectral efficiency, Error-rate, Power Amplification, Equalization Rake receiver concepts, Diversity and space-time processing, Speech coding and channel coding.

UNIT V SYSTEM EXAMPLES AND DESIGN ISSUES 09

Multiple Access Techniques – FDMA, TDMA and CDMA systems, Operational systems, Wireless networking, design issues in personal wireless systems.

TOTAL: 45

REFERENCES

1. *Feher K., **"Wireless digital communications",** PHI, New Delhi, 1995.*
2. *Rappaport T.S., **"Wireless Communications; Principles and Practice",** Prentice Hall, NJ, 1996.*
3 *Lee W.C.Y., **"Mobile Communications Engineering: Theory and Applications",** Second Edition, McGraw-Hill, New York, 1998.*
4 *Schiller, **"Mobile Communications",** Pearson Education Asia Ltd., 2000.*

P13AETE16 VISUALIZATION TECHNIQUES

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UNIT I FOUNDATIONS FOR DATA VISUALIZATION **09**

Visualization Stages-Experimental Semiotics based on Perception Gibson's Affordance theory – Model of Perceptual Processing – Types of Data.

UNIT II COMPUTER VISUALIZATION **09**

Non-Computer Visualization-Computer Visualization - Exploring Complex Information Spaces – Fisheye Views – Applications – Comprehensible Fisheye views – Fisheye views for 3D data – Non Linear Magnification – Comparing Visualization of Information Spaces- Abstraction in computer Graphics- Abstraction in user interfaces.

UNIT III MULTIDIMENSIONAL VISUALIZATION **09**

1D-2D-3D- Multiple Dimensions – trees - web Works – Data Mapping: Document Visualization – Workspaces.

UNIT IV TEXTUAL METHODS OF ABSTRACTION **09**

Graphics to pure Text- Figure Captions in Visual Interfaces – Interactive 3D illustrations with images and text – Related Work- Consistency of rendered – images and their textual labels- Architecture- Zoom techniques for illustration purpose- Interactive handling of images and text.

UNIT V COMPUTER GRAPHICS **09**

Animating non Photo realistic Computer Graphics – Interaction Facilities and High Level Support for Animation Design – Zoom Navigation in User Interfaces – Interactive Medical Illustrations – Rendering Gestural Expressions – Animating design for Simulation – Tactile Maps for Blind people – Synthetic Holography – Abstraction Versus Realism – Integrating Spatial and Non Spatial Data.

TOTAL: 45

REFERENCES

1. *Colin Ware, Morgen Kaufmen,* ***"Information Visualization Perception for Design",*** *2nd Edition, Morgan Kaufmann, 2004.*
2. *Stuart.K.Card, Jock.D.Mackinley and Ben Shneiderman,* ***"Readings in Information Visualization Using Vision to Think"****, Morgan Kaufmann Publishers, 1999.*
3. *Thomas Strothotte,* ***"Computer Visualization – Graphics Abstraction and Interactivity"****, Springer Verlag Berlin Heiderberg 1998.*
4. *S. K. Card,* ***"Information visualization",*** *In The Human-Computer Interaction Handbook, J. Jacko, A. Sears, (editors), Lawrence Erlbaum Associates; 2003.*

P13AETE17 MACHINE VISION

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UNIT I MACHINE VISION **09**

Introduction – Machine vision –Relationship to other fields –Image definitions levels of computation- Binary image processing – Thresholding Geometric properties – position – orientation –Run length encoding -Binary algorithms – Definitions - Component labeling –Size filter –Euler number –Region boundary –Area perimeter – compact Distance measures- Distance transforms – Medial axis – Thinning expanding and shrinking –morphological operators.

UNIT II REGIONS **09**

Regions and Edges - Regions segmentation – Automatic thresholding, Limitations of Histogram methods – Region representation – array representation - Hierarchical representation - Split and merge – region merging –Removing weak edges –Region splitting - split and merge – Region growing.

UNIT III EDGE DETECTION **09**

Gradient – Steps in edge deduction –Roberts operator –sober operator – pewit operator – Comparison Second derivative operator, Laplacian operator, Second derivative Image approximation – Gaussian edge Detection –Canny edge detector –Subpixel location estimation – Edge detector performance- methods of Evaluating performance – Figure of merit –Sequential methods – Line detection.

UNIT IV OPTICS SHADING **09**

Optics – lens equation –Image resolution –Depth of Field view volume –Exposure- shading – Image Inductance –Illumination – Reflector –Surface orientation –shape from shading depth – Stereo imaging –Cameras in arbitrary position and orientation –Stereo matching –Edge matching – Region correlation shape from X – Range imaging – structural lighting – Imaging Radar- Active vision.

UNIT V DYNAMIC VISION AND OBJECT RECOGNITION **09**

Change detection –Difference pictures – Static segmentation and matching –object recognition – system components – complexity of object recognition – object representation -observer -centered –object centered representations – feature detection –recognition strategies – classification – Matching Feature indexing - verification – Temperature matching –morphological approach – symbolic – analogical methods.

TOTAL: 45

REFERENCES

1. *Ramesh Jain, Rangachar Kasturi and Brian G. Schunck,* ***"Machine Vision",*** *McGraw Hill International Edition, 2006.*
2. *Anil K. Jain,* ***"Fundamentals of Digital Image Processing",*** *PHI, 2006.*
3. *Gregory A Baxes,* ***"Digital Image Processing, John Wiley & Sons",*** *1994.*
4. *W.K. Pratt,* ***"Digital Image Processing, John Wiley and Sons",*** *2001.*

P13AETE18 MACHINE LEARNING

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UNIT I INTRODUCTION **09**

Learning Problems – Perspectives and Issues – Concept Learning – Version Spaces and Candidate Eliminations – Inductive bias – Decision Tree learning – Representation – Algorithm – Heuristic Space Search.

UNIT II NEURAL NETWORKS AND GENETIC ALGORITHMS **09**

Neural Network Representation – Problems – Perceptrons – Multilayer Networks and Back Propagation Algorithms – Advanced Topics – Genetic Algorithms – Hypothesis Space Search – Genetic Programming – Models of Evolution and Learning.

UNIT III BAYESIAN AND COMPUTATIONAL LEARNING **09**

Bayes Theorem – Concept Learning – Maximum Likelihood – Minimum Description Length Principle – Bayes Optimal Classifier – Gibbs Algorithm – Naïve Bayes Classifier – Bayesian Belief Network – EM Algorithm – Probability Learning – Sample Complexity – Finite and Infinite Hypothesis Spaces – Mistake Bound Model.

UNIT IV INSTANT BASED LEARNING **09**

K- Nearest Neighbour Learning – Locally weighted Regression – Radial Bases Functions – Case Based Learning.

UNIT V ADVANCED LEARNING **09**

Learning Sets of Rules – Sequential Covering Algorithm – Learning Rule Set – First Order Rules – Sets of First Order Rules – Induction on Inverted Deduction – Inverting Resolution – Analytical Learning – Perfect Domain Theories – Explanation Base Learning – FOCL Algorithm – Reinforcement Learning – Task – Q Learning – Temporal Difference Learning

CASE STUDIES:

1. Heuristic Space Search technique
2. Genetic algorithm.
3. Learning methodologies.
4. Radial Basis Functions.

TOTAL: 45

REFERENCES

1. *Tom M. Mitchell,* ***"Machine Learning",*** *New Delhi: McGraw-Hill Science/Engineering/Math, 1997.*
2. *Ethem Alpaydin,* ***"Introduction to Machine Learning (Adaptive Computation and Machine Learning)"*** *New Delhi: The MIT Press 2004.*
3. *T. Hastie, R. Tibshirani and J. H. Friedman,* ***"The Elements of Statistical Learning",*** *New York: Springer; 2001.*
4. *Bishop, C.* ***"Pattern Recognition and Machine Learning",*** *Berlin: Springer-Verlag.2006.*

P13AETE19 PATTERN RECOGNITION AND ARTIFICIAL INTELLIGENCE

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UNIT I PATTERN CLASSIFIER **09**

Overview of pattern recognition -Discriminant functions-Supervised learning –Parametric estimation- Maximum likelihood estimation –Bayesian parameter estimation- Perceptron algorithm-LMSE algorithm – Problems with Bayes approach –Pattern classification by distance functions-Minimum distance pattern classifier

UNIT II UNSUPERVISED CLASSIFICATION **09**

Clustering for unsupervised learning and classification - Clustering concept-C-means algorithm-Hierarchical clustering procedures- Graph theoretic approach to pattern clustering - Validity of clustering solutions.

UNIT III STRUCTURAL PATTERN RECOGNITION **09**

Elements of formal grammars-String generation as pattern description - recognition of syntactic description- Parsing-Stochastic grammars and applications - Graph based structural representation.

UNIT IV FEATURE EXTRACTION AND SELECTION **09**

Entropy minimization - Karhunen-Loeve transformation-feature selection through functions approximation- Binary feature selection.

UNIT V RECENT ADVANCES **09**

Neural network structures for Pattern Recognition –Neural network based Pattern associators-Unsupervised learning in neural Pattern Recognition-Self organizing networks-Fuzzy logic-Fuzzy classifiers-Pattern classification using Genetic Algorithms.

TOTAL: 45

REFERENCES

1. *R.O Duda, P.E Hart and Strok, **"Pattern Classification",** Wiley, 2001.*
2. *Robert J. Sehalkoff, **"Pattern Recognition: Statistical, Structural and Neural Approaches",** John Wiley & Sons Inc., 2007.*
3 *Tou Gonzales, **"Pattern Recognition Principles",** Wesley Publication Company, 2000.*
4 *Morton Nadier and P. Eric Smith, **"Pattern Recognition Engineering",** John Wiley & Sons, 2000.*
5. *IEEE Transaction on Pattern Recognition Technique, 2006.*
6. *IEEE Engineering Medicine and Biology Magazine, 2006*

P13AETE20 IMAGE PROCESSING AND PATTERN RECOGNITION

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UNIT I IMAGE REPRESENTATION **09**

Principles of digital aerial photography- Sensors for aerial photography - camera mounts - Sampling, quantization, Image Basis Function, Two dimensional DFT, Discrete cosine Transform, Walsh- Hadamard transform, wavelet transform, principal component analysis.

UNIT II IMAGE ENHANCEMENT AND RESTORATION **09**

Edge Detection, Thresholding, Half toning, Median filtering, Histogram Equalization, Homomorphic filtering, PSFs for Different forms of Blur- Defocused lens with circular aperture-Uniform Motion Blur, Long-Exposure atmospheric Blur.

UNIT III IMAGE COMPRESSION **09**

Transform coding, Predictive compression methods, Vector quantization, Hierarchical and Progressive compression methods, JPEG, Video coding, Motion Estimation, MPEG-Lossless compression, Huffman coding, Run length coding and Arithmetic coding.

UNIT IV IMAGE ANALYSIS **09**

Segmentation, Thresholding, Edge based and Region based – shape representation and description – contour based and Region based texture- statistical texture description – syntactic texture description.

UNIT V PATTERN RECOGNITION **09**

Linear Discriminant Analysis- Baye's classifier – Neural net- Feed forward, unsupervised learning, Hopfield nets- fuzzy system-optimization techniques in Recognition-Genetic algorithm-Simulated annealing.

TOTAL: 45

REFERENCES

1. *Gonzalez R. C. and Woods R.E.,* ***"Digital Image Processing",*** *Prentice Hall, 2002*
2. *Jain A.K.,* ***"Fundamentals of Digital Image Processing",*** *Prentice Hall, 1989.*
3. *William K. Pratt,* ***"Digital Image Processing",*** *John Wiley, 2001.*
4. *Sonka M,* ***"Image Processing, Analysis and Machine vision",*** *Vikas Publishing Home (Thomson) 2001*
5. *Schalkoff R.J.,* ***"Digital Image Processing & Computer vision",*** *John Wiley sons, 1989.*
6. *Dudar R.O., and Hart P.E.,* ***"Pattern classification and scene Analysis",*** *2002.*

P13AETE21 IMAGE AND VIDEO PROCESSING

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UNIT I IMAGE AND VIDEO ACQUISITION **09**

Image Scanning - Sampling and Interpolation - Video Sampling and Interpolation - Image and Video Rendering and Assessment - Image Quantization - Half toning and Printing – Perceptual Criteria for Image Quality Evaluation.

UNIT II IMAGE AND VIDEO ENHANCEMENT AND RESTORATION **09**

Basic Linear and Non Linear Filtering with Applications to Image Enhancement and Image Analysis - Morphological Filtering for Image Enhancement and Detection - Basic Methods for Image Restoration and Identification.

UNIT III MULTICHANNEL IMAGE RECOVERY **09**

Multi-frame Image Restoration - Iterative Image Restoration - Motion Detection and Estimation - Video Enhancement and Restoration - Reconstruction from Multiple Images - 3-D Shape Reconstruction from Multiple Views - Images Sequence Stabilization - Mosaicking and Super-resolution.

UNIT IV IMAGE AND VIDEO ANALYSIS **09**

Image Representations and Image Models - Computational Models of Early Human Vision - Multiscale Image Decompositions and Wavelets - Random Field Models - Image Modulation Models - Image Noise Models - Color and Multispectral Image Representation and Display.

UNIT V IMAGE AND VIDEO ANALYSIS **09**

Image and Video Classification and Segmentation - Statistical Methods for Image Segmentation - Multiband Techniques for Texture Classification and Segmentation - Video Segmentation - Adaptive and Neural Methods for Image Segmentation - Edge and Boundary Detection in Images - Gradient and Laplacian Edge Detection - Diffusion-Based Edge Detectors.

TOTAL: 45

REFERENCES

1. *A.L. Bovik, "**Handbook of Image and Video Processing**", Academic Press- 2000.*
2. *Ling Guan, Sun-Yuan Kung, Jan Larsen, "**Multimedia Image and Video Processing**", CRC Press- 2001.*
3 *Stefan Winkler, "**Digital Video Quality - Vision Models and Metrics**", John Wiley and Sons Ltd, 2nd Edition.*
4. *David Bull et al, "**Video Coding for Mobile Communications**" Academic Press,2002*

P13AETE22 MIXED SIGNAL VLSI DESIGN

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UNIT I BASIC ANALOG BUILDING BLOCKS **09**

Current mirrors – Voltage sources/references – Voltage amplifiers – Transconductance and Transresistance amplifiers – Operational amplifiers – Comparators – Multipliers.

UNIT II INTRODUCTION TO ACTIVE FILTERS AND SWITCHED CAPACITOR FILTERS **09**

Active RC Filters for monolithic filer design : First and Second order filter realizations - Universal active filter (KHN) – Self tuned filter – Programmable filters – Switched capacitor filters: Switched capacitor resistors – amplifiers – comparators – sample and hold circuits – Integrator – BiQuad

UNIT III CONTINUOUS TIME FILTERS AND DIGITAL FILTERS **09**

Introduction to Gm - C filters – bipolar transconductors – CMOS Transconductors using Triode transistors, active transistors – BiCMOS transconductors – MOSFET C Filters – Tuning Circuitry – Dynamic range performance – Digital Filters: Sampling - decimation – Interpolation – Implementation of FIR and IIR filters.

UNIT IV DIGITAL TO ANALOG AND ANALOG TO DIGITAL CONVERTERS **09**

Non-idealities in the DAC – Types of DACs: Current switched, Resistive, Charge redistribution (capacitive), Hybrid, segmented DACs – Techniques for improving linearity – Analog to Digital Converters: quantization errors – non-idealities – types of ADCs: Flash, two step, pipelined, successive approximation, folding ADCs.

UNIT V SIGMA DELTA CONVERTERS **09**

Over sampled converters – Over sampling without noise and with noise – Implementation imperfections – First order modulator – Decimation filters – Second order modulator – Sigma delta DAC and ADCs, Mixed Layout**:** CMOS design rules – Layout of CMOS – BJT – Capacitors – Resistors – Mixed layout issues: Floor planning, power supply and ground, fully differential matching, Guard rings and shielding.

TOTAL: 45

REFERENCES

1. *Baker R J, Li H W, and Boyce D E, "**CMOS: Circuit Design, Layout and Simulation**", Prentice Hall of India,2005*
2. *David A Johns, Ken Martin, " **Analog Integrated Circuit Design**" John Wiley and Sons, 2005*
3. *Phillip Allen and Douglas Holmberg, "**CMOS Analog Circuit Design**", 2nd Edition, Oxford University Press, 2004*
4. *Rudy van de Plassche, "**Integrated Analog-to-Digital and Digital –to-Analog Converters**", Springer India,2005*
5. *Benhard Razavi, "**Data Converters**", Kluwer publishers, 1999*
6. *Antoniou, "**Digital filters analysis and design**", Tata McGraw Hill, New Delhi, 1998*

P13AETE23 VLSI TESTING AND TESTABILITY

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UNIT I TESTING AND TESTABLE DESIGN OF DIGITAL SYSTEMS 09

Need for testing – Logical Fault models - Fault detection and redundancy - Combinational circuits – Sequential circuits - Fault equivalence - Fault dominance – Logic simulation - Compiler driven Simulation - Event driven Simulation - Fault simulation techniques - Serial, parallel, deductive.

UNIT II TESTING FOR SINGLE STUCK AT FAULTS 09

Test generation algorithms for combinational circuits - Fault oriented ATG – D-algorithm – Examples – PODEM – Fault independent ATG - Random test generation – ATG for SSFs in sequential circuits -TG using iterative array models - Random test generation.

UNIT III DELAY TEST 09

Delay test problem – Path delay test – Transition faults – Delay test methodologies

UNIT IV ANALOG AND MIXED SIGNAL TEST 09

DSP based analog and mixed signal test – Static ADC and DAC testing methods - Model based Analog and Mixed signal Test - Analog fault models-Analog fault simulation – Analog ATPG

UNIT V DESIGN FOR TESTABILITY 09

Adhoc design for testability techniques - Controllability and Observability by means of scan registers – Storage cells for scan designs – Level Sensitive Scan Design - LSSD - Partial Scan – Boundary scan – BIST concepts and architectures

TOTAL: 45

REFERENCES

1. *Abramovici, M., Brever, A., and Friedman, D., "**Digital Systems Testing and Testable Design**", Jaico Publishing House.*
2. *Michael L Bushnell and Vishwani D Agarwal, "E**ssentials of Electronic Testing for Digital, Memory and Mixed Signal Circuits**", Springer, verlag 2000.*
3. *Stanley L Hurst "**VLSI Testing : Digital and Mixed Analogue Digital Techniques**", Institute of Electrical Engineers,1998*
4. *Xiaoqing Wen, Cheng Wen Wu and Laung Terng Wang "**VLSI Test Principles and Architectures: Design for Testability**", Cambridge University Press, 2000*
5. *Parag K Lala, "**Fault Tolerant and Fault Testable Hardware Design**" BS Publications, 2002*

P13AETE24 POWER ELECTRONICS

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UNIT I POWER ELECTRONIC DEVICES **09**

Characteristics of Power Devices- Characteristics of SCR, DIAC, TRIAC, SCS, GTO, PUJT- Power transistors-Power MOSFETS- LASCR- two transistor model of SCR- Protection of thyristors against over voltage- over current, dv/dt and di/dt -triggering circuits for SCR- R, RC, UJT- synchronizing with supply- triggering with microprocessor-forced commutation-different techniques-series and parallel operations of SCRs

UNIT II CONTROLLED RECTIFIERS **09**

AC-DC converters- Single Phase- Three Phase-half controlled and full controlled converters- waveforms of load voltage and line current under constant load current- effect of transformer leakage inductance-dual converter.

UNIT III CHOPPERS **09**

DC-DC converters- Principle of Choppers-control strategies- buck, boost &buck boost converters. AC voltage controllers- types, Principle, operation of single phase AC voltage Controllers.

UNIT IV INVERTERS **09**

Voltage and current source Inverters, Resonant, series inverter, PWM inverter.

UNIT V INDUSTRIAL APPLICATIONS **09**

DC motor Drives- Induction motor drives- Battery charger- SMPS- UPS- Induction and Dielectric Heating

TOTAL: 45

REFERENCES

1. *Mohammed H.Rashid, "**Power Electronics circuits, Devices and Applications**", third edition, PHI,2004.*
2. *M.D.Singh & K.B.Kanchandani, "**Power Electronics"** ,2nd edition, TMH,2007.*
3 *Sen "**Power Electronics**" TMH, 1987.*
4. *Dubey, " **Thyristorised Power Controllers**", Wiley Eastern 1986.*
5. *Vithayathil, "**Power Electronics- Principles and Applications**", TMH,1995*
6 *Lander, "**Power Electronics**", 3rd edition, TMH, 1994.*
7. *Jacob, "**Power Electronics**", Thomson Learning, 2002.*
8. *V.R.Moorthy, "**Power Electronics**", Oxford university Press, 2005.*

P13AETE25 DATA CONVERTERS

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UNIT I SAMPLE AND HOLD CIRCUITS 09

Sampling switches, Conventional open loop and closed loop sample and hold architecture, Open loop architecture with miller compensation, multiplexed input architectures, recycling architecture switched capacitor architecture.

UNIT II SWITCHED CAPACITOR CIRCUITS AND COMPARATORS 09

Switched-capacitor amplifiers, switched capacitor integrator, switched capacitor common mode feedback. Single stage amplifier as comparator, cascaded amplifier stages as comparator, latched comparators.

UNIT III DIGITAL TO ANALOG CONVERSION 09

Performance metrics, reference multiplication and division, switching and logic functions in DAC, Resistor ladder DAC architecture, current steering DAC architecture.

UNIT IV ANALOG TO DIGITAL CONVERSION 09

Performance metric, Flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture

UNIT V PRECISION TECHNIQUES 09

Comparator offset cancellation, Op Amp offset cancellation, Calibration techniques, range overlap and digital correction.

TOTAL: 45

REFERENCES

1. *Behzad Razavi,* ***"Principles of data conversion system design",*** *S.Chand and company ltd, 2000.*
2. *D. Johns and K. Martin,* ***"Analog Integrated Circuit Design",*** *Wiley, 1997*
3. *R. Schreier and G.C. Temes,* ***"Understanding Delta-Sigma Data Converters",*** *IEEE Press/Wiley, 2004*
4. *F. Maloberti,* ***"Data Converters",*** *Springer 2007*

P13AETE26 SYNTHESIS AND OPTIMIZATION OF DIGITAL CIRCUITS

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UNIT I CIRCUITS AND HARDWARE MODELING **09**

Design of Microelectronic Circuits - Computer Aided Synthesis and optimization-Combinatorial optimization-Boolean Algebra and Application-Hardware Modeling Languages –Compilation and Behavioral optimization.

UNIT II ARCHITECTURAL LEVEL SYNTHESIS AND OPTIMIZATION **09**

Fundamental Architectural synthesis Problems- Area and performance Estimation-Control unit synthesis-Synthesis of pipelined circuits.

UNIT III SCHEDULING ALGORITHMS AND RESOURCE SHARING **09**

Unconstrained Scheduling-ASAP Algorithm-ALAP Scheduling Algorithm- Scheduling with Resource Constraints- Scheduling pipelined circuits-Sharing and binding for Dominated circuits-Area Binding-Concurrent Binding –Module selection problems-Structural testability.

UNIT IV LOGIC-LEVEL SYNTHESIS AND OPTIMIZATION **09**

Logic optimization Principles-Algorithms and Logic Minimization –Encoding problems-Multiple-level optimization of logic networks-Algebraic and Boolean model-Algorithm for delay Evaluation-Rule based logic optimization

UNIT V SEQUENTIAL LOGIC OPTIMIZATION **09**

Sequential circuit -State Encoding-Minimization methods-Retiming- Finite state machine-testability for synchronous circuits-Algorithm for library binding- Look-Up table - FPGA- Rule-based library binding.

TOTAL: 45

REFERENCES

1. *Giovanni De Micheli,* ***"Synthesis and optimization of Digital Circuits",*** *Tata McGraw-Hill, 2003.*
2. *John Paul Shen, Mikko H. Lipasti,* ***"Modern processor Design",*** *Tata McGraw Hill, 2003*
3. *Gary D. Hachtel and Fabio Somenzi,* ***"Logic Synthesis and Verification Algorithms",*** *Springer*
4. *Frank Vahid,* ***"Digital Design",*** *John Wiley & Sons*

P13AETE27 VIRTUAL INSTRUMENTATION

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UNIT I INTRODUCTION **09**

General Functional description of a digital instrument - Block diagram of a Virtual Instrument - Physical quantities and Analog interfaces - Hardware and Software - User interfaces - Advantages of Virtual instruments over conventional instruments - Architecture of a Virtual instrument and its relation to the operating system.

UNIT II SOFTWARE OVERVIEW **09**

LabVIEW - Graphical user interfaces - Controls and Indicators - 'G' programming - Data types - Data flow programming - Editing - Debugging and Running a Virtual instrument - Graphical programming pallets - Front panel objects - Controls, Indicators, Object properties and their configuration – Typical examples.

UNIT III PROGRAMMING STRUCTURE **09**

FOR loops, WHILE loop, CASE structure, formula node, Sequence structures - Arrays and Clusters - Array operations - Bundle - Bundle/Unbundle by name, graphs and charts - String and file I/O - High level and Low level file I/O - Attribute modes Local and Global variables.

UNIT IV HARDWARE ASPECTS **09**

Installing hardware, installing drivers - Configuring the hardware - Addressing the hardware in LabVIEW - Digital and Analog I/O function - Data Acquisition - Buffered I/O - Real time Data Acquisition.

UNIT V LABVIEW APPLICATIONS **09**

Motion Control: General Applications - Feedback devices, Motor Drives – Machine vision – LabVIEW IMAQ vision – Machine vision Techniques – Configuration of IMAQ DAQ Card - Instrument Connectivity - GPIB, Serial Communication - General, GPIB Hardware & Software specifications - PXI / PCI: Controller and Chassis Configuration and Installation.

TOTAL: 45

REFERENCES

1. *Garry W Johnson, "**LabView Graphical Programming**", Tata McGraw Hill, 3rd Edition, 2001.*
2. *Sanjay Gupta and Joseph John, **"Virtual Instrumentation Using LabVIEW"**, Tata McGraw-Hill, I st Edition, 2008.*
3 *LabView: Basics I & II Manual, National Instruments, 2006*
4 *Barry Paron, **"Sensors, Transducers and LabVIEW"**, Prentice Hall , 2000.*
5. *William Buchanan and Bill Buchanan, **"Computer Basics"**, CRC Press, 2000.*

P13AETE28 WAVELETS AND MULTIRESOLUTION PROCESSING

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UNIT I INTRODUCTION **09**

Vector Spaces - properties - dot product - basis - dimension, orthogonality and orthonormality - relationship between vectors and signals - Signal spaces – concept of Convergence - Hilbert spaces for energy signals - Generalised Fourier Expansion.

UNIT II MULTI RESOLUTION ANALYSIS **09**

Definition of Multi Resolution Analysis (MRA) – Haar basis - Construction of general orthonormal MRA-Wavelet basis for MRA – Continuous time MRA interpretation for the DTWT – Discrete time MRA- Basis functions for the DTWT – PRQMF filter banks

UNIT III CONTINUOUS WAVELET TRANSFORM **09**

Wavelet Transform - definition and properties - concept of scale and its relation with frequency - Continuous Wavelet Transform (CWT) - Scaling function and wavelet functions (Daubechies, Coiflet, Mexican Hat, Sinc, Gaussian, Bi-Orthogonal) – Tiling of time -scale plane for CWT.

UNIT IV DISCRETE WAVELET TRANSFORM **09**

Filter Bank and sub band coding principles - Wavelet Filters - Inverse DWT computation by Filter banks -Basic Properties of Filter coefficients - Choice of wavelet function coefficients - Mallat's algorithm for DWT - Lifting Scheme: Wavelet Transform using Polyphase matrix Factorization – Geometrical foundations of lifting scheme - Lifting scheme in Z –domain

UNIT V APPLICATIONS **09**

Image Compression using DWT – Sequential / Progressive - JPEG 2000 standard - Image denoising - Edge detection and object Isolation and Object Detection - Image Fusion -Wavelet Packets- Multiwavelets - Non linear wavelets – Ridgelets – Curvelets – Contourlets.

TOTAL: 45

REFERENCES

1. *C. Sidney Burvus, Ramesh A.Gopinath haito , "**Introduction to wavelets and wavelet Transform",** Prentice Hall International, 1995.*
2. *Gilbert Strang, **"Linear Algebra and its Applications**", 3rd edition.*
3. *J.C. Goswami, A.K. Chan, **"Fundamentels of wavelets",** John wiley and sons, 1999.*
4. *Strang G, Nguyen T, **"Wavelets and Filter Banks,"** Wellesley Cambridge Press,1996.*
5. *Vetterli M, Kovacevic J, **"Wavelets and Sub-band Coding,"** Prentice Hall, 1995.*
6. *Mallat S., **"Wavelet Signal Processing",** Academic Press, 1996.*

P13AETE29 MULTIRATE SIGNAL PROCESSING

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UNIT I FUNDAMENTALS OF MULTIRATE SYSTEMS 09

Sampling theorem - sampling at sub nyquist rate - Basic Formulations and schemes-Multirate operations- Decimation and Interpolation - Digital Filter Banks –Interconnection of Building Blocks- Decimation with transversal filters – Interpolation with transversal filters – **Polyphase representation** -Decimation with Polyphase filters – Interpolation with polyphase filters – Decimation and Interpolation with Rational sampling factors

UNIT II MAXIMALLY DECIMATED FILTER BANKS 09

Quadrature mirror filter banks -Errors in the QMF bank- Perfect reconstruction (PR) QMF Bank - Design of an alias free QMF Bank - Biorthogonal and linear phase filter banks – Transmuliplexer filter banks

UNIT III PERFECT RECONSTRUCTION FILTER BANKS 09

Paraunitary PR Filter Banks- Filter Bank Properties induced by paraunitarity - Two channel FIR paraunitary QMF Bank- Linear phase PR Filter banks- Necessary conditions for Linear phase property- Quantization Effects: -Types of quantization effects in filter banks. - coefficient sensitivity effects, dynamic range and scaling.

UNIT IV FILTER BANKS WITH POLYPHASE STRUCTURE 09

Fundamental polyphase structures – polyphase QMF banks – General two channel polyphase filter banks – General M-channel polyphase filter banks – Paraunitary polyphase filter banks – DFT polyphase filter banks. Application: Digital audio.

UNIT V COSINE MODULATED FILTER BANKS 09

Cosine Modulated pseudo QMF Bank- Alias cancellation- Elimination of Phase distortion- Closed form expression- Cosine modulated PR Systems-Sub band coding of speech and Image signals

TOTAL: 45

REFERENCES

1. *Vaidyyanathan P P, "**Multirate Systems and Filter Banks",** Prentice Hall Inc., 2011*
2. *Fliege N J, "**Multirate Digital Signal Processing",** John Wiley and sons, 1994*
3 *J.G. Proakis. D.G. Manolakis. **"Digital Signal Processing: Principles. Algorithms and Applications",** 3rd Edn.Prentice Hall India, 1999*
4 *Sanjit K Mitra, "**Digital Signal Processing-A Computer Based Approach",** Tata McGraw Hill, 2003*
5. *R.E. Crochiere. L. R. **"Multirate Digital Signal Processing",** Prentice Hall. Inc.1983.*

P13AETE30 MULTIMEDIA COMPRESSION TECHNIQUES

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UNIT I INTRODUCTION **09**

Multimedia data - features — Storage requirements for multimedia - Need for Compression - Taxonomy of compression – Metrics – Quantitative and Qualitative techniques - Overview of source coding – Scalar quantization - Adaptive - Vector quantization.

UNIT II TEXT COMPRESSION **09**

Characteristics of text data – RLE, Huffmann coding – Adaptive Huffmann Coding – Arithmetic coding — Dictionary techniques – static and adaptive- digram coding – LZW algorithm - GIF, TIF, Digitized documents, JBIG, JBIG2.

UNIT III AUDIO COMPRESSION **09**

Fundamental concepts of digital audio - Audio compression techniques –μ Law and A- Law companding - PCM, DPCM, DM, ADM - sub-band coding – Application to speech coding – G.722 – MPEG audio – MP3 - Dolby audio - Model based coding – Channel Vocoders – LPC - Formant and CELP coders.

UNIT IV IMAGE COMPRESSION **09**

Image data representation - Predictive techniques – DPCM: Optimal Predictors and Optimal Quantizers –Transform Coding – JPEG Standard – Sub-band coding – QMF Filters - Wavelet based compression – EZW, SPIHT coders – JPEG 2000 standard – File formats.

UNIT V VIDEO COMPRESSION **09**

Fundamental concepts of video – digital video signal - video formats – video compression techniques and standards - AVI, FLV, MP4, Real media - Motion estimation and compensation Techniques, Block matching- Full search motion estimation methods – MPEG Video Coding : MPEG – 1 and 2, MPEG – 4, 7 and 21 — H.26X Standard - Packet Video.

TOTAL: 45

REFERENCES

1. *Khalid Sayood, **" Introduction to Data Compression",** Morgan Kauffman Harcourt India, 2nd Edition, 2000.*
2. *David Salomon, **" Data Compression – The Complete Reference",** Springer Verlag New York Inc., 2nd Edition, 2001.*
3 *I.E.G. Richardson, **"Video codec design",** John Wiley & Sons Ltd, 2002 Edition.*
4 *Yun Q.Shi, Huifang Sun, **" Image and Video Compression for Multimedia Engineering - Fundamentals, Algorithms & Standards",** CRC press, 2003.*
5. *Peter Symes , **"Digital Video Compression",** McGraw Hill Pub., 2004.*
6. *Mark Nelson , **"Data compression",** BPB Publishers, New Delhi,1998.*
7. *Mark S.Drew, Ze-Nian Li, **" Fundamentals of Multimedia",** PHI, 1st Edition, 2003.*
8. *Watkinson,J, **" Compression in Video and Audio",** Focal press,London.1995.*
9. *Jan Vozer , **"Video Compression for Multimedia",** AP Profes, NewYork, 1995*

P13COTE23 SPEECH AND AUDIO SIGNAL PROCESSING

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UNIT I MECHANICS OF SPEECH **09**

Speech production mechanism – Nature of Speech signal – Discrete time modelling of Speech production – Representation of Speech signals – Classification of Speech sounds – Phones – Phonemes – Phonetic and Phonemic alphabets – Articulatory features.

Music production – Auditory perception – Anatomical pathways from the ear to the perception of sound – Peripheral auditory system – Psycho acoustics

UNIT II TIME DOMAIN METHODS FOR SPEECH PROCESSING **09**

Time domain parameters of Speech signal – Methods for extracting the parameters Energy, Average Magnitude – Zero crossing Rate – Silence Discrimination using ZCR and energy – Short Time Auto Correlation Function – Pitch period estimation using Auto Correlation Function

UNIT III FREQUENCY DOMAIN METHODS FOR SPEECH PROCESSING **09**

Short Time Fourier analysis – Filter bank analysis – Formant extraction – Pitch Extraction – Analysis by Synthesis- Analysis synthesis systems- Phase vocoder – Channel Vocoder. Homomorphic speech analysis: Cepstral analysis of Speech – Formant and Pitch Estimation – Homomorphic Vocoders.

UNIT IV LINEAR PREDICTIVE ANALYSIS OF SPEECH **09**

Formulation of Linear Prediction problem in Time Domain – Basic Principle – Auto Correlation method – Covariance method – Solution of LPC equations – Cholesky Method – Durbin's Recursive algorithm – lattice formation and solutions – Comparison of different methods – Application of LPC parameters – Pitch detection using LPC Parameters – Formant analysis – VELP – CELP.

UNIT V APPLICATIONS OF SPEECH & AUDIO SIGNAL PROCESSING **09**

Algorithms: Spectral Estimation, dynamic time warping, hidden Markov model – Music analysis – Pitch Detection – Feature analysis for recognition – Music synthesis – Automatic Speech Recognition – Feature Extraction for ASR – Deterministic sequence recognition – Statistical Sequence recognition – ASR systems – Speaker identification and verification – Voice response system – Speech Synthesis: Text to speech, voice over IP.

TOTAL: 45

REFERENCES

1. *Ben Gold and Nelson Morgan, **"Speech and Audio Signal Processing",** John Wiley and Sons Inc, Singapore, 2004.*
2. *L.R.Rabiner and R.W.Schaffer, **"Digital Processing of Speech signals"**, Prentice Hall -1978.*
3 *Quatieri, **"Discrete-time Speech Signal Processing",** Prentice Hall, 2001.*
4 *J.L.Flanagan, **" Speech analysis: Synthesis and Perception",**2nd edition, Berlin,1972.*
5. *I.H.Witten, **" Principles of Computer Speech"**, Academic Press,1982.*

P13AETE31 ROBOTICS

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UNIT I INTRODUCTION **09**

Motion - Potential Function, Road maps, Cell decomposition and Sensor and sensor planning. Kinematics. Forward and Inverse Kinematics - Transformation matrix and DH transformation. Inverse Kinematics - Geometric methods and Algebraic methods. Non-Holonomic constraints.

UNIT II COMPUTER VISION **09**

Projection - Optics, Projection on the Image Plane and Radiometry. Image Processing - Connectivity, Images-Gray Scale and Binary Images, Blob Filling, Thresholding, Histogram. Convolution - Digital Convolution and Filtering and Masking Techniques. Edge Detection - Mono and Stereo Vision.

UNIT III SENSORS AND SENSING DEVICES **09**

Introduction to various types of sensor. Resistive sensors. Range sensors – Ladar (laser distance and ranging), Sonar, Radar and Infra-red, Introduction to sensing - Light sensing, Heat sensing, Touch sensing and Position sensing.

UNIT IV ARTIFICIAL INTELLIGENCE **09**

Uniform Search strategies - Breadth first, Depth first, Depth limited, Iterative and deepening depth first search and Bidirectional search. The A* algorithm, Planning - State-Space, Plan-Space Planning, Graphplan/ SatPlan and their Comparison, Multi-agent planning 1 and Multi-agent planning 2, Probabilistic Reasoning - Bayesian Networks, Decision Trees and Bayes net inference

UNIT V INTEGRATION TO ROBOT **09**

Building of 4 axis and 6 axis robot - Vision System for pattern detection - Sensors for obstacle detection - AI algorithms for path finding and decision making.

TOTAL: 45

REFERENCES

1. *Duda, Hart and Stork**, "Pattern Recognition",** Wiley-Interscience, 2000.*
2. *Mallot, **"Computational Vision: Information Processing in Perception and Visual Behavior."** Cambridge, MA: MIT Press, 2000.*
3 *Stuart Russell and Peter Norvig, **"Artificial Intelligence-A Modern Approach",** Pearson Education Series in Artificial Intelligence, 2004*
4 *I.H.Witten, **" Principles of Computer Speech"**, Academic Press,1982.*
5. *Robert Schilling and Craig, **"Fundamentals of Robotics, Analysis and control",** Prentice Hall of India Private Limied, New Delhi, 2003.*
6. *Forsyth and Ponce **,"Computer Vision, A modern Approach ",** Person Education 2003.*

P13AETE32 MICRO ELECTROMECHANICAL SYSTEMS

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UNIT I INTRODUCTION TO MEMS **09**

MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Micro accelorometers and Micro fluidics, MEMS materials, Micro fabrication.

UNIT II MECHANICS FOR MEMS DESIGN **09**

Elasticity, Stress, strain and material properties, Bending of thin plates, Spring configurations, torsional deflection, Mechanical vibration, Resonance, Thermo mechanics – actuators, force and response time, Fracture and thin film mechanics.

UNIT III ELECTRO STATIC DESIGN AND SYSTEM ISSUES **09**

Electrostatics: basic theory, electro static instability. Surface tension, gap and finger pull up, Electro static actuators, Comb generators, gap closers, rotary motors, inch worms, Electromagnetic actuators. bistable actuators. Electronic Interfaces, Feedback systems, Noise, Circuit and system issues.

UNIT IV MEMS APLLICATION **09**

Case studies – Capacitive accelerometer, Peizo electric pressure sensor, Microfluidics application, Modeling of MEMS systems, CAD for MEMS.

UNIT V INTRODUCTION TO OPTICAL AND RF MEMS **09**

Optical MEMS, - System design basics – Gaussian optics, matrix operations, resolution. Case studies, MEMS scanners and retinal scanning display, Digital Micro mirror devices. RF Memes – design basics, case study – Capacitive RF MEMS switch, performance issues.

TOTAL: 45

REFERENCES

1. *Stephen Santeria, **"Microsystems Design",** Kluwer publishers, 2000.*
2. *N.P.Mahalik, **"MEMS",**Tata McGraw hill, 2007*
3. *Nadim Maluf, **" An introduction to Micro electro mechanical system design"**, Artech House, 2000.*
4. *Mohamed Gad-el-Hak, editor, **" The MEMS Handbook",** CRC press Baco Raton,2000.*
5. *Tai Ran Hsu, **" MEMS & Micro systems Design and Manufacture"** Tata McGraw Hill, New Delhi, 2002.*
6. *Liu, **"MEMS",** Pearson education, 2007.*

P13AETE33 ADVANCED PROCESSORS

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UNIT I MICROPROCESSOR ARCHITECTURE 09

Instruction set – Data formats – Instruction formats – Addressing modes – Memory hierarchy – register file – Cache – Virtual memory and paging – Segmentation – Pipelining – The instruction pipeline – pipeline hazards – Instruction level parallelism – reduced instruction set – Computer principles – RISC versus CISC – RISC properties – RISC evaluation.

UNIT II HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM 09

The software model – functional description – CPU pin descriptions – Addressing modes – Processor flags – Instruction set – Bus operations – Super scalar architecture – Pipe lining – Branch prediction – The instruction and caches – Floating point unit– Programming the Pentium processor.

UNIT III HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM INTERFACE 09

Protected mode operation – Segmentation – paging – Protection – multitasking – Exception and interrupts - Input /Output – Virtual 8086 model – Interrupt processing.

UNIT IV HIGH PERFORMANCE RISC ARCHITECTURE: ARM 09

ARM architecture – ARM assembly language program – ARM organization and implementation – ARM instruction set - Thumb instruction set .

UNIT V SPECIAL PURPOSE PROCESSORS 09

Altera Cyclone Processor – Audio codec – Video codec design – Platforms – General purpose processor – Digital signal processor – Embedded processor – Media Processor – Video signal Processor – Custom Hardware – Co-Processor.

TOTAL: 45

REFERENCES

1. *Daniel Tabak, **"Advanced Microprocessors",** McGraw Hill.Inc., 1995.*
2. *James L. Antonakos, **"The Pentium Microprocessor",** Pearson Education, 1997.*
3. *Steve Furber, **"ARM System –On –Chip architecture",**Addison Wesley, 2000.*
4. *Gene .H.Miller, **"Micro Computer Engineering",** Pearson Education, 2003.*
5. *Barry.B.Brey, **"The Intel Microprocessors Architecture, Programming and Interfacing",** PHI, 2002.*
6. *Valvano, "**Embedded Microcomputer Systems**" Thomson Asia PVT LTD first reprints, 2001.*
7. *Iain E.G.Richardson, **"Video codec design",** John Wiley & sons Ltd, U.K, 2002.*

P13AETE34 PROCESS CONTROL

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UNIT I MATHEMATICAL MODELLING OF PROCESSES **09**

Need for process control – Mathematical model of first order liquid level and thermal processes – Higher order process – Process with dead time, process with inverse response – Interacting and non-interacting systems – Continuous and batch process – Servo and regulator operation.

UNIT II CONTROLLER CHARACTERISTICS & TUNING **09**

Basic control action – Characteristics of ON-OFF, proportional, integral and derivative control modes – Composite control modes – P+I, P+D and P+I+D control modes – Electronic controllers to realize various control actions – Evaluation criteria – IAE, ISE, ITAE and ¼ decay ratio – Tuning of controllers – Ziegler-Nichol's and Cohencoon method – Damped oscillation method.

UNIT III CONTROL SYSTEMS WITH MULTIPLE LOOPS **09**

Cascade control – Feed forward control – Ratio control – Selective control systems – Split range control – Adaptive and inferential control.

UNIT IV FINAL CONTROL ELEMENT **09**

I/P converter – Pneumatic and electric actuators – Valve positioner – Control valve characteristics – Classification of control valves – Control valve sizing – Cavitation and flashing – Selection of control valves.

UNIT V SELECTED UNIT OPERATIONS **09**

Mixing – Evaporation – Drying – Heat exchanger – Distillation process – Case study of control schemes of binary distillation column.

TOTAL: 45

REFERENCES

1. *Donald P. Eckman, **'Automatic Process Control'**, Wiley Eastern Ltd., New Delhi, 1993.*
2. *G. Stephanopoulis, **'Chemical Process Control'**, Prentice Hall of India, New Delhi, 1990.*
3. *B.G. Liptak, **'Process Control'**, Chilton Book Company, 1994.*
4. *Curtis D. Johnson, **'Process Control Instrumentation Technology'**, 7th Edition, Pearson Education, New Delhi, 2002.*

P13AETE35 EMBEDDED SYSTEMS IN AUTOMOTIVE APPLICATIONS

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UNIT I AUTOMOBILE ELECTRICAL AND ELECTRONICS 09

Basic Electrical Components and their operation in an automobile - Starting systems, Charging systems – ignition systems- Electronic fuel control- Environmental legislation for pollution- Overview of vehicle electronic systems- Power train subsystem- chassis subsystem- comfort and safety subsystems.

UNIT II INTRODUCTION TO EMBEDDED SYSTEMS 09

Embedded Systems definition - Components of Embedded systems – Microprocessor - Classification of Microprocessors- Microcontrollers- Memory - Peripherals. Introduction to an embedded board (TMS470 based / ARM9 based) for hands on lab sessions (RISC processor based with standard peripherals / interfaces and I/Os)

UNIT III OPERATING SYSTEM IN EMBEDDED ENVIRONMENT 09

Introduction to OS - General Purpose OS, RTOS -, Kernel - Pre-emptive & Non pre-emptive, Scheduler, Interrupt - Interrupt latency and Context Switch Latency- Board Support package, Task - Multi-tasking, Task synchronization, Inter-task communication, Features of a typical embedded RTOS (µC/OS-II)

UNIT IV INTEGRATED DEVELOPMENT ENVIRONMENT 09

Integrated Development Environment (IDE)- Getting Started, Hardware / Software Configuration (Boot Service, Host – Target Interaction), Booting, Reconfiguration, Managing IDE, Target Servers, Agents, Cross – Development, debugging- Introduction to an IDE for the lab board – RTOS, PC based debugger.

UNIT V COMMUNICATION PROTOCOLS AND APPLICATIONS 09

Engine Management systems - Diesel / Gasoline systems, Various sensors used in system - Vehicle safety systems- electronic control of braking and traction- Introduction to control elements and control methodology- Electronic transmission control- Body electronics - Infotainment systems – Navigation systems- Introduction to CAN, LIN, FLEXRAY, MOST, KWP 2000 Protocols

TOTAL: 45

REFERENCES

1. *R. K. Jurgen, "**Automotive electronics handbook"** McGraw Hill Professional, 1999*
2. *Paul Pop, Petru Eles, Zebo Peng **"Analysis and Synthesis of Distributed Real-Time Embedded Systems"** Springer, 21-Dec-2004*
3. *B. Kanta Rao **"Embedded Systems"** PHI Learning Pvt. Ltd.2011*

P13AETE36 ADVANCED EMBEDDED DEVELOPMENT

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UNIT I EMBEDDED REAL TIME SYSTEMS & PROCESSOR ARCHITECTURE **09**

Introduction to Embedded real time systems - Soft Real Time systems, Hard Real Time systems, Embedded hard wares – Microprocessors, Micro controllers, Peripheral Interfaces. Processor architectures- Single core, Multi core.

UNIT II REAL TIME OPERATING SYSTEMS & COMMUNICATION PROTOCOLS **09**

Real time operating systems- Introduction to RTOS- Single core architectures - Multi core architectures - Hypervisor systems

Embedded systems communication protocols - On Board communication – SPI, I2C. - Automotive vehicle communication – LIN, CAN, FlexRay, Ethernet, MOST.

UNIT III EMBEDDED DEVELOPMENT TOOLS **09**

Embedded Development Tools - Automotive s/w architecture – AUTOSAR- Model based approach for embedded software development - ASCET - Matlab/Simulink. - IDE –Integrated Development Environments - Automatic code generation- Simulators/Emulators, Debug Interfaces

UNIT IV EMBEDDED SYSTEMS IN AUTOMOTIVE APPLICATIONS **09**

Embedded systems in Automotive applications: Power train Applications, Engine Control Module, and Transmission Control Module - Vehicle Applications: Body Control Module, Infotainment, Chassis, Airbag, and Cruise. - Driver Assistance Systems: Lane departure warning, ACC

UNIT V EMBEDDED SYSTEMS SAFETY & SECURITY, CRYPTOGRAPHY **09**

Safety - Introduction to Embedded Safety – Active/Passive safety - Automotive safety applications (SRS) – ABS, Airbags, Cruise control. -Overview of IEC61508/ISO26262 - Security- Introduction to IT security - Challenges of embedded security (which is quite different due to space/timing constraints) - Security building blocks such as hardware (e.g., Smart cards) and software (such as crypto library etc.).

TOTAL: 45

REFERENCES

1. *Jörg Schäuffele, Thomas Zurawka* ***"Automotive Software Engineering: Principles, Processes, Methods, And Tools",*** *PublisherSAE International*
2. *Wolfgang Ecker, Wolfgang Müller, Rainer. Dömer,* ***"Hardware-dependent Software",*** *Springer, 01-Jan-2009 - Computers*
3. *Hermann Kopetz,* ***"Real-time Systems: Design Principles for Distributed Embedded Applications",*** *Second Edition, Springer Publications*
4. *Nicolas Navet, Francoise Simonot-Lion,* ***"Automotive Embedded Systems Handbook",*** *CRC Press, 20-Dec-2008 - Technology & Engineering*

P13AETE37 SYSTEM MODELING AND SIMULATION

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UNIT I SIMULATION **09**

Introduction – Systems, Models and Simulation- Application areas – Model Classification- Types of Simulation- Discrete Event Simulation – Distributed Simulation --Monte Carlo Simulation- Steps in a Simulation Study- Review of Probability and Statistics.

UNIT II MATHEMATICAL MODELS **09**

Statistical Models - Concepts – Discrete Distributions- Continuous Distributions – Poisson Process- Empirical Distributions - Queuing Models– Characteristic Notation - Queuing Systems – Markovian Models- Properties of Random Numbers-Generation of Pseudo Random Numbers- Techniques for generating random numbers-Testing random number generators- Generating Random Variates - Inverse Transform Technique - Acceptance- Rejection Technique – Composition and Convolution Method.

UNIT III ANALYSIS OF SIMULATION DATA **09**

Input Modeling - Data collection - Assessing sample independence – Hypothesizing distribution family with data - Parameter Estimation- Goodness-of-fit tests – Selecting input models in absence of data- Output analysis for a Single system –Terminating Simulations – Steady state simulations.

UNIT IV VERIFICATION AND VALIDATION **09**

Building – Verification of Simulation Models – Calibration and Validation of Models – Validation of Model Assumptions – Validating Input – Output Transformations.

UNIT V SIMULATION SOFTWARE AND CASE STUDIES **09**

Simulation Tools –Simulation Languages–Classification of Simulation Software –Desirable Software Features– GPSS/H– SIMAN– SIMSCRIPT II.5– SLAM II and Related Software – Comparison of Simulation Languages and General Purpose Languages – Case studies.

TOTAL: 45

REFERENCES

1. *Jerry Banks and John Carson, **"Discrete Event System Simulation",** Fourth Edition, PHI, 2005.*
2. *Geoffrey Gordon, **"System Simulation",** Second Edition, PHI, 2006.*
3. *Frank L. Severance, **"System Modeling and Simulation",** Wiley, 2001.*
4. *Averill M. Law and W.David Kelton, **"Simulation Modeling and Analysis",** Third Edition, McGraw Hill, 2006.*
5. *Jerry Banks, **"Handbook of Simulation: Principles, Methodology, Advances, Applications and Practice"**, Wiley-Interscience, 1 edition, 1998.*

P13COTE24 RESEARCH METHODOLOGY

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UNIT I RESEARCH CONCEPTS **09**

Concepts, meaning, objectives, motivation, types of research, approaches, research (Descriptive research, Conceptual, Theoretical, Applied & Experimental). Formulation of Research Task – Literature Review, Importance & Methods, Sources, quantification of Cause Effect Relations, Discussions, Field Study, Critical Analysis of Generated Facts, Hypothetical proposals for future development and testing, selection of Research task.

UNIT II MATHEMATICAL MODELING AND SIMULATION **09**

Concepts of modeling, Classification of Mathematical Models, Modeling with Ordinary differential Equations, Difference Equations, Partial Differential equations, Graphs, Simulation, Process of formulation of Model based on Simulation.

UNIT III EXPERIMENTAL MODELING **09**

Definition of Experimental Design, Examples, Single factor Experiments, Guidelines for designing experiments. Process Optimization and Designed experiments, Methods for study of response surface, determining optimum combination of factors, Taguchi approach to parameter design.

UNIT IV ANALYSIS OF RESULTS **09**

Parametric and Non-parametric, descriptive and Inferential data, types of data, collection of data (normal distribution, calculation of correlation coefficient), processing, analysis, error analysis, different methods, analysis of variance, significance of variance, analysis of covariance, multiple regression, testing linearity and non-linearity of model.

UNITV REPORT WRITING **09**

Types of reports, layout of research report, interpretation of results, style manual, layout and format, style of writing, typing, references, tables, figures, conclusion, appendices.

TOTAL: 45

REFERENCES

1. *R. Panneerselvam, **"Research Methodology"**, PHI 2004.*
2. *Douglas Montgomary, **"Design of Experiments, Statistical Consulting Services",** 1990.*
3. *Douglas H. W. Allan, **"Statistical Quality Control: An Introduction for Management",** Reinhold Pub Corp, 1959.*
4. *Cochran and Cox, **"Experimental Design",** John Willy & Sons, 2nd Edition , May 1992*
5. *S. S. Rao, **"Optimization Theory and Application",** Wiley Eastern Ltd., New Delhi, 1996.*
6. *C. R. Kothari, **"Research Methodology",** New Age Publishers, 2005.*