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ELECTRICAL AND ELECTRONICS ENGINEERING

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M.E. EMBEDDED SYSTEM

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KUMARAGURU COLLEGE OF TECHNOLOGY,
COIMBATORE – 641 049
(An Autonomous Institution Affiliated To Anna University Chennai)

ELECTRICAL AND ELECTRONICS ENGINEERING

VISION

The Vision of the Department is to be a Centre of Excellence in Globalizing Power Engineering and Technology.

MISSION

The mission of the department is to Empower Youth by Imparting Technical Knowledge and Skills to Innovate, Transform and Globalize the Power Sector. It intended to equip the graduates with deftness to overcome challenges culminating in success in diverse competitive careers with societal impacts and values.

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Kumaraguru College of Technology
Coimbatore – 641 049
Regulations 2015

CBCS – PG Curriculum

Name of the PG Programme: Embedded System Technologies

Foundation Courses (FC)

S. No.	Course Code	Course Title	Periods/Wk & Credits				Preferred Semest
			L	T	P	C	
1.	P15MAT106	Applied Mathematics for Embedded Systems	3	1	0	4	1

Professional Core (PC)

S. No.	Course Code	Course Title	Periods /Wk & Credits				Preferred Semest
			L	T	P	C	
1.	P15EST101	Advanced Digital System Design	3	0	0	3	1
2.	P15EST102	Embedded Systems Design	3	0	0	3	1
3.	P15EST103	Real Time Systems	3	0	0	3	1
4.	P15EST104	Micro controller Based System	3	0	0	3	1
5.	P15EST201	Real Time Operating Systems	3	0	0	3	2
6.	P15EST202	Embedded Control Systems	3	0	0	3	2
7.	P15EST203	Embedded Processors	3	0	0	3	2
8.	P15EST204	VHDL	3	0	0	3	2
9.	P15EST205	DSP For Embedded System	3	0	0	3	2

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17.	P15ESTE16	DSP Integrated Circuits	3	0	0	3	

Professional Electives (PE)

S. No.	Course Code	Course Title	Periods / Wk & Credits				Preferr Semest
			L	T	P	C	
1.	P15ESTE01	Industrial Automation And Control	3	0	0	3	
2.	P15ESTE02	Digital Control Systems	3	0	0	3	
3.	P15ESTE03	Solid State Converters	3	0	0	3	
4.	P15ESTE04	Intelligent Control	3	0	0	3	
5.	P15ESTE05	Industrial Robotics and Expert Systems	3	0	0	3	
6.	P15ESTE06	Micro Electro Mechanical Systems	3	0	0	3	
7.	P15ESTE07	System Simulation and Modeling	3	0	0	3	
8.	P15ESTE08	Advanced Computer Architecture	3	0	0	3	
9.	P15ESTE09	Software Technology for Embedded Systems	3	0	0	3	
10.	P15ESTE10	Operating Systems	3	0	0	3	
11.	P15ESTE11	Advanced Embedded Systems	3	0	0	3	
12.	P15ESTE12	Embedded Networking	3	0	0	3	
13.	P15ESTE13	Embedded Sensor Networks	3	0	0	3	
14.	P15ESTE14	Embedded Control of Electrical Drives	3	0	0	3	
15.	P15ESTE15	Digital Image Processing	3	0	0	3	
16.	P15PETE17*	Advanced Digital Signal Processing	3	0	0	3	

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18.	P15ESTE17	Embedded Communication software design	3	0	0	3	
19.	P15ESTE18	Data Communication and Networks	3	0	0	3	
20.	P15ESTE19	Wireless and Mobile Communication	3	0	0	3	
21.	P15ESTE20	VLSI Architecture and Design Methodologies	3	0	0	3	
22.	P15ESTE21	VLSI Design	0	0	0	3	
23.	P15ESTE22	ASIC and FPGA Design	0	0	0	3	

Employability Enhancement Courses (EEC)

S. No.	Course Code	Course Title	Periods /Wk & Credits				Preferred Semester
			L	T	P	C	
1.	P15ESP101	Embedded System Laboratory I	0	0	4	2	1
2.	P15ESP201	Embedded System Laboratory II	0	0	4	2	2
3.	P15ESP301	Embedded System Laboratory III	0	0	4	2	3
4.	P15ESP302	Project (Phase-I)	0	0	12	6	3
5.	P15ESP401	Project (Phase II)	0	0	24	12	4

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SEMESTER I

S. No.	Course Code	Course Title	Category	Contact Hours	L	T	P	C
Theory								
1.	P15MAT106	Applied Mathematics for Embedded Systems	FC	4	3	1	0	4
2.	P15EST101	Advanced Digital System Design	PC	3	3	0	0	3
3.	P15EST102	Embedded Systems Design	PC	3	3	0	0	3
4.	P15EST103	Real Time Systems	PC	3	3	0	0	3
5.	P15EST104	Micro controller Based System Design	PC	3	3	0	0	3
6.	E1	Elective I	PE	3	3	0	0	3
Practical								
7.	P15ESP101	Embedded System Laboratory I	EEC	4	0	0	4	2
								Total Credits: 21

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SEMESTER II

S. No.	Course Code	Course Title	Category	Contact Hours	L	T	P	C
Theory								
1.	P15EST201	Real Time Operating Systems	PC	3	3	0	0	3
2.	P15EST202	Embedded Control Systems	PC	3	3	0	0	3
3.	P15EST203	Embedded Processors	PC	3	3	0	0	3
4.	P15EST204	VHDL	PC	3	3	0	0	3
5.	P15EST205	DSP For Embedded System	PC	3	3	0	0	3
6.	E2	Elective II	PE	3	3	0	0	3
Practical								
7.	P15ESP201	Embedded System Laboratory II	EEC	4	0	0	4	2
								Total Credits: 20

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SEMESTER III

S. No.	Course Code	Course Title	Category	Contact Hours	L	T	P	C
Theory								
1.	E3	Elective III	PE	3	3	0	0	3
2.	E4	Elective IV	PE	3	3	0	0	3
3.	E5	Elective V	PE	3	3	0	0	3
4.	S1	Self study	PE	3	0	0	0	3
Practical								
5.	P15ESP301	Embedded System Laboratory III	EEC	4	0	0	4	2
6.	P15ESP302	Project (Phase I)	EEC	12	0	0	12	6
								Total Credits: 20

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SEMESTER IV

S. No.	Course Code	Course Title	Category	Contact Hours	L	T	P	C
Practical								
7.	P15ESP401	Project (Phase II)	EEC	24	0	0	24	12
								Total Credits: 12

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ELECTIVES

S. No.	Course Code	Course Title	Category	Contact Hours	L	T	P	C
Specialization 1 ** Automation and Control								
1.	P15ESTE01	Industrial Automation And Control	PE	3	3	0	0	3
2.	P15ESTE02	Digital Control Systems	PE	3	3	0	0	3
3.	P15ESTE03	Solid State Converters	PE	3	3	0	0	3
4.	P15ESTE04	Intelligent Control	PE	3	3	0	0	3
5.	P15ESTE05	Industrial Robotics and Expert Systems	PE	3	3	0	0	3
6.	P15ESTE06	Micro Electro Mechanical Systems	PE	3	3	0	0	3
7.	P15ESTE07	System Simulation and Modeling	PE	3	3	0	0	3
Specialization 2 ** Embedded Software								
8.	P15ESTE08	Advanced Computer Architecture	PE	3	3	0	0	3
9.	P15ESTE09	Software Technology for Embedded Systems	PE	3	3	0	0	3
10.	P15ESTE10	Operating Systems	PE	3	3	0	0	3
Specialization 3 ** Embedded System								
11.	P15ESTE11	Advanced Embedded Systems	PE	3	3	0	0	3
12.	P15ESTE12	Embedded Networking	PE	3	3	0	0	3
13.	P15ESTE13	Embedded Sensor	PE	3	3	0	0	3

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		Networks						
14.	P15ESTE14	Embedded Control of Electrical Drives	PE	3	3	0	0	3
Specialization 4 ** Signal Processing								
15.	P15ESTE15	Digital Image Processing	PE	3	3	0	0	3
16.	P15PETE17 *	Advanced Digital Signal Processing	PE	3	3	0	0	3
17.	P15ESTE16	DSP Integrated Circuits	PE	3	3	0	0	3
Specialization 5 ** Embedded Communication								
18.	P15ESTE17	Embedded Communication software design	PE	3	3	0	0	3
19.	P15ESTE18	Data Communication and Networks	PE	3	3	0	0	3
20.	P15ESTE19	Wireless and Mobile Communication	PE	3	3	0	0	3
Specialization 6 ** VLSI								
21.	P15ESTE20	VLSI Architecture and Design Methodologies	PE	3	0	0	0	3
22.	P15ESTE21	VLSI Design	PE	3	0	0	0	3
23.	P15ESTE22	ASIC and FPGA Design	PE	3	0	0	0	3

Total Credits: 73

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ONE CREDIT COURSES			
S. No.	**Course Code**	**Course Title**	**Industry that will offer the course**
1.	P15ESIN01	Internet of Things	Robert Bosch
2.	P15ESIN02	Embedded system in Cars	Robert Bosch
3.	P15ESIN03	Advanced Communication PROTOCOLS	TP Vision India Pvt. Ltd.,
4.	P15ESIN04	PLC Based Automation in Industries	Axis Global Automation

*** Common Elective subject for Power Electronics and Drives & Embedded System Technologies.**

**** All electives should be only in category PE**

***** Grouping of electives according to specialization is optional**

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SEMESTER I

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ELECTRICAL AND ELECTRONICS ENGINEERING
M.E – EMBEDDED SYSTEM TECHNOLOGIES
REGULATIONS 2015
SYLLABUS

P15MAT106	APPLIED M ATHEMATICS FOR EMBEDDED SYSTEMS	L	T	P	C
		3	1	0	4

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Apply the Laplace transform to solve initial and boundary value problems.

CO2: Understand the series solution and its role in Bessel Functions and Legendre Polynomials.

CO3: Know the basic concepts and differences between Discrete Fourier transform and Z- transform.

CO4: Construct probabilistic models for observed phenomena through distributions which play an important role in many engineering applications.

CO5: Choose a class of models in which customers arrive in some random manner at a service facility.

PRE-REQUISITE

1. NIL

THE WAVE EQUATION 9+3 Hours

Solution of initial and boundary value problems – Characteristics – D'Alembert's Solution – Significance of Characteristic curves – Laplace transform solutions for displacement in a long string – a long string under its weight – a bar with prescribed force on one end – free vibration of a string.

SPECIAL FUNCTIONS 9+3 Hours

Series solutions – Bessel's equation – Bessel Functions – Legendre's

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equation – Legendre Polynomials – Rodrigue's formula – Recurrence relations – Generating Functions and orthogonal property for Bessel functions of the first kind – Legendre Polynomials.

FOURIER ANALYSIS AND Z –TRANSFORMS 9+3 Hours

Discrete Fourier Transforms and its properties – Fourier series and its properties – Fourier representation of finite duration sequences – Z-transform – Properties of the region of convergence – Inverse Z-transform – Z-transform properties.

PROBABILITY AND RANDOM VARIABLES 9+3 Hours

Probability – Random variables – Binomial, Poisson, Geometric, Uniform, Normal, Exponential distributions – Moment generating functions and their properties – Functions of Random variables.

QUEUING THEORY 9+3 Hours

Queuing characteristics, single server and parallel server models:

(M / M / 1): $(\infty / FIFO)$, (M / M / k): $(\infty / FIFO)$, (M / M / 1): $(N / FIFO)$, (M / M / k): $(N / FIFO)$ M/G/1 queuing system – P-K formula**.**

Theory:45 Hrs Tutorial: 15 Hrs Total: 60 Hrs

REFERENCES

1. Andrews L.C., and Shivamoggi, "B.K. Integral Transforms for Engineers", Prentice Hall of India Pvt. Ltd, New Delhi, 2003.
2. Gupta, S.C and Kapoor V.K., "Fundamentals of Mathematical Statistics", Sultan Chand and sons, New Delhi, 2001.
3. Taha H A, "Operations Research: An Introduction", Pearson Education Edition, Asia, New Delhi, Seventh Edition 2002.
4. O'Neil P.V., "Advanced Engineering Mathematics", Thomson Brooks/Cole, Singapore, 5th Edition, 2003.
5. Andrews L.C., "Special Functions of Mathematics for Engineers", McGraw Hill, Inc., Singapore, 2nd Edition, 1992.

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P15EST101 **ADVANCED DIGITAL SYSTEM DESIGN**

L	T	P	C
3	0	0	3

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Analyze and design the Clocked synchronous sequential circuits and asynchronous sequential circuits for a digital circuit.

CO2: To study about different types of faults and testability algorithms.

CO3: To explain about features of VHDL language and design a digital system using VHDL.

PRE-REQUISITE

1. Digital System Design

SEQUENTIAL CIRCUIT DESIGN 9 Hours

Analysis of Clocked Synchronous Sequential Networks (CSSN) Modeling of CSSN – State Stable Assignment and Reduction – Design of CSSN – Design of Iterative Circuits – ASM Chart – ASM Realization.

ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9 Hours

Analysis of Asynchronous Sequential Circuit (ASC) – Flow Table Reduction – Races in ASC – State Assignment – Problem and the Transition Table – Design of ASC – Static and Dynamic Hazards – Essential Hazards – Data Synchronizers – Designing Vending Machine Controller – Mixed Operating Mode Asynchronous Circuits.

FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9 Hours

Fault Table Method – Path Sensitization Method – Boolean Difference Method – Kohavi Algorithm – Tolerance Techniques – The Compact Algorithm – Practical PLA's – Fault in PLA – Test Generation – Masking Cycle – DFT Schemes – Built-in Self Test.

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SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES **9 Hours**

EPROM to Realize a Sequential Circuit – Programmable Logic Devices – Designing a Synchronous Sequential Circuit using a GAL – EPROM – Realization State machine using PLD – FPGA – Xilinx FPGA – Xilinx 2000 - Xilinx 3000.

SYSTEM DESIGN USING VHDL **9 Hours**

VHDL Description of Combinational Circuits – Arrays – VHDL Operators – Compilation and Simulation of VHDL Code – Modelling using VHDL – Flip Flops – Registers – Counters – Sequential Machine – Combinational Logic Circuits - VHDL Code for – Serial Adder, Binary Multiplier – Binary Divider – complete Sequential Systems – Design of a Simple Microprocessor.

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1. Donald G. Givone, "Digital principles and Design", 1st Edition, Tata McGraw Hill, 2012.
2. Charles H. Roth Jr., "Digital System Design using VHDL", 2nd Edition, Cengage Learning, 2007.
3. Navabi.Z, "VHDL Analysis and Modeling of Digital Systems", McGraw International, 1992.
4. Parag K Lala, "Digital System design using PLD" 1st Edition BS Publications, 2003.
5. Skahill. K, "VHDL for Programmable Logic" Pearson Education, 1996.
6. Robert K Dueck, "Digital Design with CPLD applications and VHDL", Thomson Asia, 2004.

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P15EST102 **EMBEDDED SYSTEMS DESIGN**

L	T	P	C
3	0	0	3

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Outline the basic concepts of embedded system.

CO2: Acquire the knowledge of PIC controller and its computing platform.

CO3: Describe and distinguish various software development tools.

PRE-REQUISITE

1. Embedded Processors

EMBEDDED SYSTEM DESIGN 9 Hours

Embedded systems descriptions & definitions – Challenges - Embedded system design considerations and requirements, processor selection and tradeoffs - Overview of board development process – Configurable / Reconfigurable Embedded Systems - Hardware /Software co verification- Microprocessor / Microcontroller.

DESIGN USING PIC MICROCONTROLLER 9 Hours

CPU Architecture and instruction set – Program and Data memory – CPU registers – IO port expansion – External Interrupts and Timers – RB0/INT – Timer0 – Compare and Capture mode – Timer 1 – PWM outputs – I2C operation – ADC – UART.

EMBEDDED COMPUTING PLATFORM 9 Hours

CPU bus- Memory devices- I/O devices- Component interfacing- Designing with Microprocessors- Development and Debugging- Design example- Design patterns- Dataflow graphs- Assembly and Linking- Basic compilation techniques- Analysis and Optimization.

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DISTRIBUTED EMBEDDED SYSTEM DESIGN 9 Hours

Inter-process communication- Signals – Shared memory Communication- Accelerated design- Design for video accelerator- Networks for embedded systems- Networks based design- Internet enabled systems - Embedded Design methodologies and tools – design flows – designing hardware and software components - requirement analysis and specification.

SOFTWARE DEVELOPMENT AND TOOLS 9 Hours

Embedded system evolution trends - Round Robin, robin with Interrupts, function-One-Scheduling Architecture, Algorithms-Introduction to-assembler-compiler-cross compilers and Integrated Development Environment (IDE)-Object Oriented Interfacing, Recursion, Debugging strategies, Simulators-Logic Analyzers - ICD and ICE. (MPLAB IDE Programming).

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1. Raymond J.A.Bhur and Donald L.Bialey, "An Introduction to Real Time Systems: From Design to Networking with C/C++", Prentice Hall, 1999, New Jersey.
2. Wayne Wolf, "Computers as Components: Principles of Embedded Computing System Design", Morgan Kaufman Publishers, 2008.
3. David E Simon, "An Embedded Software Primer ", Pearson Education Asia, 2001
4. John B. Peatman, "Design with PIC microcontrollers", Pearson Education, 1998, Singapore.
5. Tim Wilmshurst, "Designing Embedded Systems with PIC Microcontrollers: Principles and Applications", Newnes Publisher, 2010.

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P15EST103

REAL TIME SYSTEMS

L	T	P	C
3	0	0	3

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Summarize the basics and importance of real-time systems.

CO2: List the use of multi-task scheduling algorithms in real-time systems and task, Databases scheduling.

CO3: Outline the features and structures of practical implementations of Network Topologies and ability to solve the real-time systems problems.

PRE-REQUISITE

1. Real Time Operating Systems
2. Operating Systems

REAL TIME SYSTEMS 9 Hours

Introduction – Issues in Real Time Computing, Structure of a Real Time System, Task classes, Performance Measures for Real Time Systems, Estimating Program Run Times. Task Assignment and Scheduling – Classical uniprocessor scheduling algorithms, Uniprocessor scheduling of IRIS tasks, Task assignment, Mode changes, and Fault Tolerant Scheduling.

PROGRAMMING LANGUAGES AND TOOLS 9 Hours

Programming Languages and Tools – Desired language characteristics, Data typing, Control structures, Facilitating Hierarchical Decomposition, Packages, Run – time (Exception) Error handling, Overloading and Generics, Multitasking, Low level programming, Task Scheduling, Timing Specifications, Programming Environments, Run – time support.

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REAL TIME DATABASES **9 Hours**

Real time Databases – Basic Definition, Real time Vs General Purpose Databases, Main Memory Databases, Transaction priorities, Transaction Aborts, Concurrency control issues, Disk Scheduling Algorithms, Two – phase Approach to improve Predictability, Maintaining Serialization Consistency, Databases for Hard Real Time Systems.

COMMUNICATION **9 Hours**

Real Time Communication – Communications media, Network Topologies Protocols, Fault Tolerant Routing. Fault Tolerance Techniques – Fault Types, Fault Detection. Fault Error containment Redundancy, Data Diversity, Reversal Checks, Integrated Failure handling.

EVALUATION TECHNIQUES **9 Hours**

Reliability Evaluation Techniques – Obtaining parameter values, Reliability models for Hardware Redundancy, Software error models. Clock Synchronization – Clock, A Nonfault – Tolerant Synchronization Algorithm, Impact of faults, Fault Tolerant Synchronization in Hardware, Fault Tolerant Synchronization in software.

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1. C.M. Krishna, Kang G. Shin, "Real – Time Systems", McGraw Hill, 2005.
2. Stuart Bennett, "Real Time Computer Control – An Introduction", Prentice Hall of India, 2000.
3. Peter D.Lawrence, "Real Time Micro Computer System Design – An Introduction", McGraw Hill, 1988.
4. S.T. Allworth and R.N.Zobel, "Introduction to real time software design", 2nd Edition, Macmillan, 2005.
5. R.J.A Buhur, D.L Bailey, "An Introduction to Real – Time Systems", Prentice Hall of India, 2002.

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P15EST104	MICROCONTROLLER BASED SYSTEM DESIGN	L	T	P	C
		3	0	0	3

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Describe the Architecture, Instruction sets and peripherals of the 8051 and PIC Microcontroller.

CO2: Write programs for 8051 and PIC Microcontroller to interfacing the peripheral devices.

CO3: Design an Embedded system.

PRE-REQUISITE

1. Microprocessors and Architecture

8051 ARCHITECTURE 9 Hours

Architecture – memory organization – addressing modes – instruction set – Timers - Interrupts - I/O ports, Interfacing I/O Devices – Serial Communication.

8051 PROGRAMMING 9 Hours

Assembly language programming – Arithmetic Instructions – Logical Instructions –Single bit Instructions – Timer Counter Programming – Serial Communication Programming Interrupt Programming – RTOS for 8051 – RTOS Lite – Full RTOS –Task creation and run – LCD digital clock/thermometer using Full RTOS.

PIC MICROCONTROLLER 9 Hours

Architecture – memory organization – addressing modes – instruction set – PIC programming in Assembly & C –I/O port, Data Conversion, RAM & ROM Allocation, Timer programming, MP-LAB.

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PERIPHERAL OF PIC MICROCONTROLLER **9 Hours**

Timers – Interrupts, I/O ports- I2C bus-A/D converter-UART- CCP modules -ADC, DAC and Sensor Interfacing –Flash and EEPROM memories.

SYSTEM DESIGN – CASE STUDY **9 Hours**

Interfacing LCD Display – Keypad Interfacing - Generation of Gate signals for converters and Inverters - Motor Control – Controlling AC appliances –Measurement of frequency - Stand alone Data Acquisition System.

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1 Muhammad Ali Mazidi, Rolin D. Mckinlay, Danny Causey, "PIC Microcontroller and Embedded Systems using Assembly and C for PIC18", Pearson Education, 2008.

2 John Iovine, "PIC Microcontroller Project Book", McGraw Hill, 2004.

3 Myke Predko, "Programming and customizing the 8051 microcontroller", Tata McGraw Hill 2001.

4 Michael Slater, "Microprocessor based designs a comprehensive guide to effective Hardware design" Prentice Hall, 1989, New Jersey.

5 Ayala, Kenneth, "The 8051 Microcontroller" Delmar Cengage Learning, 2004.

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P15ESP101	EMBEDDED SYSTEM LABORATORY - I	L	T	P	C
		0	0	4	2

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Write Input output interfacing programs for 8051 and PIC Microcontrollers

CO2: Write Interrupt / Timer programs for 8051 and PIC Microcontrollers

CO3: Design an embedded system by interfacing peripherals like ADC, LCD, Keypad, Switches, timer and counter applications

PRE-REQUISITE

1. Embedded Processors

LIST OF EXPERIMENTS:

8051 Micro controller

IO Programming

1. Write an Embedded C program to read a switch connected to a port and make a LED to glow connected a another port after a delay.
2. Write an assembly language input output program using 8051 microcontroller for given task.
3. Write an Embedded C program to generate Analog waveforms using 8051 microcontroller.
4. Write an Embedded C program for timer and interrupts application using 8051 microcontroller.
5. Write an Embedded C program to interface LCD with 8051 microcontroller to display the given characters.

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6. Write an Embedded C program to interface ADC with 89C51 microcontroller.
7. Write an Embedded C program using Arrays and Pointers in 8051, C compiler.

PIC Micro controller

IO Programming

8. Introduction to Software Tools MPLAB, PROTEUS, and QL-2006 programmer.
9. Delay Loops Applications Flasher & Counter.

Interrupts and Timer application

10. TMR0 Application Counter Using TMR0.
11. Interrupt Application Controlling flashing speed of a flasher.
12. EEPROM Memory Application.

Interfacing Experiments

13. Application for Keypad and LCD.
14. Analog Digital Conversion.
15. Pulse-width modulation (PWM).

RTOS

16. Task schedule using Micrium OS – II

Experiments beyond the syllabus should be conducted

Practical:45 Hrs **Total: 45 Hrs**

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SEMESTER II

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P15EST201 **REAL TIME OPERATING SYSTEMS**

L	T	P	C
3	0	0	3

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Familiarity with key Real-Time Operating System terms and concepts.

CO2: Comprehend and ability to use tools to build an embedded real-time system.

CO3: Ability to specify, design and implement a small embedded system.

PRE-REQUISITE

1. Real Time Systems

REVIEW OF OPERATING SYSTEMS 9 Hours

Basic Principles – System Calls – Files – Processes – Design and Implementation of processes – Communication between processes – Operating System structures.

DISTRIBUTED OPERATING SYSTEMS 9 Hours

Topology – Network types – Communication – RPC – Client server model – Distributed file system – Design strategies.

REAL TIME MODELS AND LANGUAGES 9 Hours

Event Based – Process Based and Graph based Models – Petrinet Models – Real Time Languages – RTOS Tasks – RT scheduling - Interrupt processing – Synchronization – Control Blocks – Memory Requirements.

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REAL TIME KERNEL **9 Hours**

Principles – Design issues – Polled Loop Systems – RTOS Porting to a Target – Comparison and study of various RTOS like QNX – VX works – PSOS – C Executive – Case studies.

RTOS APPLICATION DOMAINS **9 Hours**

RTOS for Image Processing – Embedded RTOS for voice over IP – RTOS for fault Tolerant Applications – RTOS for Control Systems.

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1. Hermann Kopetz, "Real Time Systems – Design Principles for Distributed Embedded Applications", Springer Science & Business Media, 2011.
2. Charles Crowley, "Operating Systems-A Design Oriented approach" McGraw Hill, 2005.
3. C.M. Krishna, Kang, G.Shin, "Real Time Systems", Tata McGraw Hill, 2010.
4. Raymond J.A.Bhur, Donald L.Bailey, "An Introduction to Real Time Systems", Prentice Hall of India, 2006.
5. Intel Manual on 16 bit embedded controllers, Santa Clara, 2005.

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P15EST202 **EMBEDDED CONTROL SYSTEMS**

L	T	P	C
3	0	0	3

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Describe the basics and importance of real-time systems hardware with software.

CO2: Demonstrate the interfacing of I/O Devices and Communication devices.

CO3: Write Embedded C programming for practical implementations of motors and ability to solve the problems in embedded systems.

PRE-REQUISITE

1. Embedded Processors
2. Microcontroller Based System Design

CONTROL OF HARDWARE AND SOFTWARE 6 Hours

Controlling the hardware with software – Data lines – Address lines - Ports – Schematic representation – Bit masking – Programmable peripheral interface –Switch input detection – 74 LS 244.

INPUT-OUTPUT DEVICES 8 Hours

Keyboard basics – Keyboard scanning algorithm – Multiplexed LED displays – Character LCD modules – LCD module display – Configuration – Time-of-day clock– Timer manager - Interrupts - Interrupt service routines – IRQ - ISR – Interrupt vector or dispatch table multiple-point - Interrupt-driven pulse width modulation.

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D/A AND A/D CONVERSION **12 Hours**

R 2R ladder - Resistor network analysis - Port offsets - Triangle waves analog vs. digital values - ADC0809 – Auto port detect - Recording and playing back voice - Capturing analog information in the timer interrupt service routine - Automatic, multiple channel analog to digital data acquisition.

ASYNCHRONOUS SERIAL COMMUNICATION **9 Hours**

Asynchronous serial communication – RS-232 – RS-485 – Sending and receiving data – Serial ports on PC – Low-level PC serial I/O module - Buffered serial I/O.

CASE STUDIES: EMBEDDED C PROGRAMMING **10 Hours**

Multiple closure problems – Basic outputs with PPI – Controlling motors – Bidirectional control of motors – H bridge – Telephonic systems – Stepper control –Inventory control systems.

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1 Jean J. Labrosse, "Embedded Systems Building Blocks: Complete and Ready- To-Use Modules in C", Paul Temme, 2000.
2 Staartor, Ball P.E, "Embedded Microprocessor Systems – Real World Design", Newnes Publications, 2002.
3 Hermann Kopetz, "Real Time Systems – Design Principles for Distributed Embedded Applications", Springer Science & Business Media, 2011.
4 Daniel W. Lewis, "Fundamentals of Embedded Software where C and Assembly meet", Prentice Hall of India, 2002.

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P15EST203 **EMBEDDED PROCESSORS**

L	T	P	C
3	0	0	3

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Describe the functional requirements of the hardware and software components of ARM processor Families.

CO2: Recall the instruction set and able to write program for DSP applications.

CO3: Outline the Black fin processor in all aspects.

PRE-REQUISITE

1. Advanced Embedded System
2.

ARM EMBEDDED SYSTEMS 9 Hours

ARM Embedded Systems – Design Philosophy –Systems Hardware – Systems Software – ARM processor fundamentals – ARM processor families.

ARM PROGRAMMING 9 Hours

ARM Instruction Set – The Thumb Instruction Set- Exception and Interrupt handling – Firmware - Example programs with embedded operating system for ARM.

ARM DSP 9 Hours

ARM Digital Signal Processing – Introduction to DSP on the ARM – FIR – IIR – DFT Exception and Interrupt Handling ARM Memory Managements Unit.

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BLACKFIN PROCESSOR **9 Hours**

Introduction to BLACKFIN processor : Embedded Processor – Micro signal Architecture – Real time embedded signal processing - Architecture – Software tools –Number formats - Overview of signal acquisition and transfer to memory- DMA operations - Using cache – Scratchpad memory of BLACKFIN processor- power management.

PRACTICAL DSP APPLICATIONS **9 Hours**

Overview of Real time processing - Signal generator with Blackfin processor -Implementation of FIR – IIR filters – Graphic equalizer - Audio coding and audio effects – Digital Image processing.

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1. Bary B. Brey, "The Intel Microprocessors Architecture, Programming and Interfacing", Prentice Hall of India, 2006, New Delhi.
2. Andrew Sloss, Dominic Symes, and Chris Wright, "ARM System Developer's Guide: Designing and Optimizing System", Morgan Kaufmann Series, 2004.
3. Woon-Seng Gan ,Sen M. Kuo, "Embedded Signal Processing with the Micro Signal Architecture" John Wiley & sons, 2007, New Jersey.
4. Jason Andrews, "Co-verification of Hardware and Software for ARM SoC Design (Embedded Technology)", Newnes Publications, 2004.

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P15EST204 **VHDL**

L	T	P	C
3	0	0	3

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Acquire the VLSI concepts and VHDL constructs.

CO2: Acquire the knowledge of programming structure of simple design and modeling concepts.

CO3: Familiarize sub programming, packages and files of VHDL.

PRE-REQUISITE

1. Digital System Design

VHDL FUNDAMENTALS 9 Hours

Fundamental Concepts – Modeling Digital Systems – Domains and Levels of Modeling – Modeling Languages – VHDL Modeling concepts – Scalar Data Types and Operations – Constants and variables – Scalar Types – Type Classification – Attributes and Scalar types – Expressions and operators – Sequential Statements – If statements – Case statements – Null Statements – Loop statements – Assertion and Report statements.

COMPOSITE DATA TYPES AND BASIC MODELING CONSTRUCTS 9 Hours

Arrays – Unconstrained Array types – Array Operations and Referencing – Records – Basic Modeling Constructs – Entity Declarations – Architecture Bodies – Behavioral Descriptions – Structural Descriptions – Design Processing. Case Study: A pipelined Multiplier Accumulator.

SUBPROGRAMS AND PACKAGES 9 Hours

Procedures – Procedure Parameters – Concurrent Procedure Call Statements – functions – Overloading – Visibility of Declarations – Packages and Use Clauses – Package declarations – Package bodies – Use

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Clauses – The predefined – Aliases - Aliases for data objects – Aliases for Non-Data Items. Case Study: A Bit-Vector Arithmetic Package.

SIGNALS, COMPONENTS, CONFIGURATIONS 9 Hours

Basic Resolved signals – IEEE Std_Logic_1164 Resolved subtypes – Resolved signal parameters – Generic Constants – Parameterizing behavior – Parameterizing structure – Components and Configurations – Components – Configuring component Instances – Configuration Specification – Generate Statements – Generating iterative structure – Conditionally generating structures – Configuration of generate Statements. Case Study: The DLX Computer System.

ADTs AND FILES 9 Hours

Access Types – Linked Data structures – Abstract Data Types using Packages – Files and Input/Output – Files – The Package Textio – Verilog. Case Study: Queuing Networks.

Theory:45 Hrs Total: 45 Hrs

REFERENCES

1. Peter J. Ashenden, "The Designer's Guide to VHDL", 3rd Edition, Morgan Kaufmann Publishers, 2008, San Francisco.
2. Zainalabedin Navabi, "VHDL Analysis and Modeling of Digital Systems", 2nd Edition, McGraw Hill International Editions, 1998.
3. James M.Lee, "Verilog Quick start", 3rd Edition, Kluwer Academic Publishers, 2002.

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P15EST205 **DSP FOR EMBEDDED SYSTEM**

L	T	P	C
3	0	0	3

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Learn the various types of signal and signal conversion techniques.

CO2: Acquire the knowledge of transformation of the signal and analyze the spectrum.

CO3: Describe the architecture of DSP and design digital and analog filters.

PRE-REQUISITE

1. Digital Signal Processing

SIGNALS AND REPRESENTATION 9 Hours

Classification of systems: Continuous, discrete, linear, causal, stable, dynamic, recursive, time variance; classification of signals: continuous and discrete, energy and power; mathematical representation of signals; spectral density; sampling techniques, quantization, quantization error, Nyquist rate, aliasing effect. Digital signal representation, analog to digital conversion.

DISCRETE TIME SYSTEM ANALYSIS 9 Hours

Z-transform and its properties, inverse z-transforms; difference equation – Solution by z-transform, application to discrete systems - Stability analysis, frequency response – Convolution – Fourier transform of discrete sequence.

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DISCRETE FOURIER TRANSFORM & COMPUTATION **9 Hours**

DFT properties, magnitude and phase representation - Computation of DFT using FFT algorithm – DIT & DIF - FFT using radix 2 – Butterfly structure.

DESIGN OF DIGITAL FILTERS **9 Hours**

FIR & IIR filter realization – Parallel & cascade forms. FIR design: Windowing Techniques – Need and choice of windows – Linear phase characteristics. IIR design: Analog filter design - Butterworth and Chebyshev approximations; digital design using impulse invariant and bilinear transformation - Warping, prewarping - Frequency transformation.

PROGRAMMABLE DSP CHIPS **9 Hours**

Architecture and features of Black fin Processor - Real-Time DSP Fundamentals and Implementation Considerations - Memory System and Data Transfer - Code Optimization

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1. D.H. Hayes, “Digital Signal Processing”, Schaum’s Outline Series, Tata McGraw Hill, 2009, New Delhi.
2. B. Venkataramani, M. Bhaskar, “Digital Signal Processors, Architecture, Programming and Applications”, Tata McGraw Hill, 2003, New Delhi.
3. J.G. Proakis and D.G. Manolakis, “Digital Signal Processing Principles, Algorithms and Applications”, Pearson Education, 2003, New Delhi.
4. Alan V. Oppenheim, Ronald W. Schafer and John R. Buck, “Discrete – Time Signal Processing”, Pearson Education, 2003, New Delhi.
5. Woon-Seng Gan, Sen.M. Kuo, “Embedded Signal Processing with the Micro Signal Architecture”, John Willey Publications, 2006.

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P15ESP201	EMBEDDED SYSTEM LABORATORY II	L	T	P	C
		0	0	4	2

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: ability to design, implement, and evaluate an embedded-based system, process, component, or program to meet desired needs.

CO2: ability to analyze a problem, and identify the computing requirements appropriate to its solution.

CO3: ability to design I/O programming, ADC/DAC, Timers, Interrupts.

PRE-REQUISITE

1. Embedded Processors
2. VHDL

LIST OF EXPERIMENTS:

1. Write a program to demonstrate I/O operation of ARM kit using LED.
2. Write a program to interface seven segment displays to ARM kit.
3. Write a program to interface LCD to ARM kit.
4. Write an ALP to find the GCD (Greatest Common Divisor), with and without conditional execution of ARM instructions.
5. Write a program to multiply two matrices with and without MLA instruction.
6. Write a program to scan the keypad, assign own values to the keys and display the key pressed.
7. Write a program for convolution of two sequences with and without MLA instruction.
8. I/O programming, ADC/DAC, Timers, Interrupts.

Design with Programmable Logic Devices using Xilinx/Altera FPGA and CPLD. Design and Implementation of simple Combinational/Sequential Circuits.

Experiments beyond the syllabus should be conducted

Practical :45 Hrs **Total: 45 Hrs**

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SEMESTER III

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P15ESP301	EMBEDDED SYSTEM LABORATORY III	L	T	P	C
		0	0	4	2

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Write DSP programs using CCS

CO2: Demonstrate the programs in TMS320C6713 kits

CO3: Develop a mini project

PRE-REQUISITE

1. Digital Signal Processing

LIST OF EXPERIMENTS:

Write DSP program for TMS320C6713 using CCS

1. Correlation,
2. Convolution,
3. Arithmetic adder,
4. Multiplier,
5. Design of Filters – FIR based , IIR based
6. Implementation of IPC mechanism using Micruim OS – II - RTOS
7. Hardware project **(using any one controller – 8051, PIC, ARM, FPGA, DSP)**

Experiments beyond the syllabus should be conducted

Practical :45 Hrs **Total: 45 Hrs**

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ELECTIVE I

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P15ESTE01	INDUSTRIAL AUTOMATION AND CONTROL	L	T	P	C
		3	0	0	3

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Demonstrate proficiency in automation programming/troubleshooting related to programmable logic controllers and digital controllers required for industrial employment.

CO2: Demonstrate problem solving skills used in ladder logic for development of industrial automation.

CO3: Students will be acquainted with knowledge of CNC based automated systems for case studies of various industries.

PRE-REQUISITE

1. NIL

INTRODUCTION TO INDUSTRIAL AUTOMATION 9 Hours

Fundamentals of Industrial Automation and Control Elements- Principles and Strategies - Smart Sensors, Transducers and Motion Actuators- PID Controller- Digital Controller. Program of Instructions.

PROGRAMMABLE LOGIC CONTROLLERS 9 Hours

Process Controller- Relay Logic – Programmable Logic Controller- Basic Structure –Ladder Logic- Programming- PLC Internal Operation and Signal Processing- I/O Processing- Remote Access- Communication System for Industrial Automation- Intelligent System for Monitoring, Supervision and Control.

COMPUTER NUMERIC CONTROL 9 Hours

Introduction to CNC Systems- Types –Analogue, Digital, Absolute and Incremental- Open Loop and Closed Loop - CNC Drives and Feedback Devices- Adaptive Control – CNC Part Programming.

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AUTOMATED SYSTEMS **9 Hours**

Fixed Automation – Programmable Automation – Flexible Automation - Material Transport Systems – Process Monitoring – Conveyor Systems – Cranes and Hoists – Automated Storage and Retrieval Systems – Automated Data Capture – Digital Factories.

INDUSTRIAL APPLICATIONS **9 Hours**

Industrial Control Applications - Cement Plant – Thermal Plant- Water Treatment Plant- Steel Plant- Irrigation Canal Management- Paper Industry.

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1. Krishna Kant, "Computer-Based Industrial Control", 2nd Edition, Prentice Hall of India, 2010, New Delhi.
2. Gray Dunning, "Introduction to Programmable Logic Controllers", Delmar Publishers, 2005.
3. Frank D. Petruzella, "Programmable Logic Controllers", 3rd Edition, Tata McGraw Hill, 2010.
4. Richard L.Shell, Ernest L.Hall, "Hand Book of Industrial Automation", Published by Marcel Dekker Inc., Society of Manufacturing Engineers, 2009.
5. Mikell P. Groover, "Automation, Production Systems and Computer Integrated Manufacturing", 3rd Edition, Prentice Hall, 2008.

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P15ESTE02 **DIGITAL CONTROL SYSTEMS**

L	T	P	C
3	0	0	3

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Students will have the knowledge of Z- Transform.

CO2: To understand the stability analysis of digital control system.

CO3: To explain the digital process control design and concepts of state space.

PRE-REQUISITE

1. Course on Control System

MODELLING OF DIGITAL SYSTEM 9 Hours

Types of signal – digital control systems – block diagram – quantization and quantization error – review of Z transform and its applications – Pulse transfer function – block diagrams – signal flow graphs – ZOH and its characteristics.

ANALYSIS OF DIGITAL CONTROL SYSTEMS 9 Hours

Mapping of s plane and z plane – steady error analysis – root locus – polar plot – Nyquist stability criterion – Bode diagram – gain and phase – margins – Jury's stability test.

DESIGN OF DIGITAL CONTROL SYSTEM 9 Hours

Design of continuous controllers with equivalent digital controllers – realization of digital controllers by digital programming – digital PID controller – design through Bilinear transformation – design in Z plane using root locus diagram – phase lead, phase lag, networks, PID, PD PI controllers.

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STATE SPACE ANALYSIS OF DIGITAL CONTROL SYSTEMS **9 Hours**

Concept of state space – state space representations of discrete systems – canonical forms – state transition matrix – properties – solution to homogeneous and non- homogeneous state equations.

POLE PLACEMENT AND OBSERVER DESIGN **9 Hours**

Controllability and observability of linear time invariant discrete systems – transforming state –space equations into canonical forms – design using pole placement – state observer – design of full order and reduced order state observers.

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1. M.Gopal, "Digital Control Engineering", 2nd Edition, New Age International, 2014.
2. Katsuhiko Ogata, "Discrete-Time Control Systems", 2nd Edition, Pearson Education, 2015.
3. Benjamin C. Kuo, "Digital Control Systems", 2nd Edition, Oxford University Press, 2012.
4. Gene F.Franklin J.David Powell and Michael Workman, "Digital Control of Dynamic Systems", 3rd Edition, Addision Wesley, 2005.
5. Charles L. Phillips and H. Troy Nagle, "Digital Control System Analysis and Design", 4th Edition, Prentice Hall, 2014.

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P15ESTE03 **SOLID STATE CONVERTERS**

L	T	P	C
3	0	0	3

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Compare the concepts and analysis the AC-DC converters.

CO2: Students able to acquire the knowledge of analysis of DC-DC converters.

CO3: Students familiarize the various types and detailed analysis of inverters.

PRE-REQUISITE

1. Power Electronics

SINGLE PHASE AC-DC CONVERTER 9 Hours

Uncontrolled, half controlled and fully controlled converters with R-L, R-L-E loads and freewheeling diodes – continuous and discontinuous models of operation – inverter operation – Dual converter - Sequence control of converters – performance parameters: harmonics, ripple, distortion, power factor – effect of source impedance and overlap.

THREE PHASE AC-DC CONVERTER 9 Hours

Uncontrolled and fully controlled – converter with R, R-L, R-L-E - loads and freewheeling diodes – inverter operation and its limit – dual inverter – performance parameters – effect of source impedance and over lap.

DC-DC CONVERTERS 9 Hours

Principles of step-down and step-up converters – Analysis of buck, boost, buck-boost and Cuk converters – time ratio and current limit control – Full bridge converter – Resonant and quasi – resonant converters.

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SINGLE PHASE INVERTERS **9 Hours**

Principle of operation of half and full bridge inverters – Performance parameters – Voltage control of single phase inverters using various PWM techniques – various harmonic elimination techniques – forced commutated Thyristor inverters.

THREE PHASE VOLTAGE SOURCE INVERTERS **9 Hours**

180 degree and 120 degree conduction mode inverters with star and delta connected loads – voltage control of three phase inverters.

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1. Ned Mohan, Tore. M. Undeland, William. P. Robbins, "Power Electronics: Converters, Applications and Design", 3rd Edition, Wiley, 2010, India.
2. M.H. Rashid, "Power Electronics: Circuits, Devices and Applications", 3rd Edition, Pearson Education, 2014, New Delhi.
3. P. C Sen., "Modern Power Electronics", 1st Edition, Wheeler publishing Co, 1998, New Delhi.
4. Jai P. Agrawal, "Power Electronics Systems", 2nd Edition, Pearson Education, 2002.
5. P.S. Bimbra, "Power Electronics", Khanna Publishers, 2012, New Delhi.
6. Bimal K. Bose. "Modern Power Electronics and AC Drives", 2nd Edition, Prentice Hall of India, 2005.

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P15ESTE04 **INTELLIGENT CONTROL**

L	T	P	C
3	0	0	3

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Describes various soft computing required for developing intelligent systems.

CO2: Outlines the concept of ANN and genetic algorithm and its role in modelling system behaviour.

CO3: Applies the knowledge of fuzzy logic techniques to analyze the system behaviour with the support of development tools.

PRE-REQUISITE

1. System Simulation and Modeling

SYSTEMS AND APPROACHES 9 Hours

Architecture of intelligent control –Knowledge representation-Expert systems. Hard computing - soft computing – features of hart and soft computing- Hybrid computing – optimization and some Traditional Methods – Drawbacks of Traditional optimization Methods.

ARTIFICIAL NEURAL NETWORKS 9 Hours

Introduction-Biological Neuron – Artificial Neuron – Neuron Modelling – learning rules – Single layor – Multilayer feed forward Network – Back Propagation – learning faction – Feedback Network – Hopfield network-Neural network based controller-Application of ANN.

FUZZY LOGIC SYSTEM 9 Hours

Crisp sets – Fuzzy sets – Fuzzy relations – Fuzzification – Defuzzification – Fuzzy rules – Membership function – Fuzzy Controller for non linear systems-Applications of FLC.

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GENETIC ALGORITHM **9 Hours**

Basic concepts – Working Principle – Encoding – Fitness function – reproduction – cross over – Mutation – Convergence of genetic Algorithms – Application of GA.

IMPLEMENTATION OF GA,NN AND FUZZY USING MATLAB TOOL BOX **9 Hours**

Genetic Algorithm application to optimization problem using GA Tool box-Implementation of fuzzy controller using MATLAB tool box- Control of linear and non linear system by neural network controller using MATLAB tool box.

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1. Jacek.M.Zurada, "Introduction to Artificial Neural Systems", Jaico Publishing House, 2012.
2. Kosko, B. "Neural Networks and Fuzzy Systems", Prentice Hall International, 2007.
3. Klir G.J. & Folger T.A. "Fuzzy sets, uncertainty and Information", Prentice Hall of India, 2003.
4. Zimmermann H.J. "Fuzzy set theory-and its Applications", Kluwer Academic Publishers, 2004.
5. Sivanandam S. N., Deepa S. N, "Introduction to Genetic Algorithms", Springer, 2008.

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P15ESTE05	INDUSTRIAL ROBOTICS AND EXPERT SYSTEMS	L	T	P	C
		3	0	0	3

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Describe the robotic drives control and cell design.

CO2: Know the mechanical parameters of the robot and its sensors and vision systems.

CO3: Design or write the coding for robot using artificial intelligence and expert systems.

PRE-REQUISITE

1. Industrial Automation and Control
2. Microcontroller Based System Design

ROBOTIC KINEMATICS AND DYNAMICS 9 Hours

Introduction to robotic kinematics- Definition, need and scope of industrial robot-Robot anatomy-Work volume-Precision movement-End effectors-Sensors, robot kinematics- Direct and inverse kinematics- Robot trajectories- Control of robot manipulations- Robot dynamics- Methods for orientation and location of objects.

ROBOT DRIVES AND CONTROL 9 Hours

Controlling the robot motion- Position and velocity sensing devices-Design of drivers of drives system- Hydraulic and pneumatic and linear and rotary actuators and control valves- Electro hydraulic servo valves, electric drives- Motors- designing of end effectors- Vacuum, magnetic and air operated grippers.

ROBOT SENSORS AND VISION SYSTEM **9 Hours**

Transducers and sensors- Sensors in robot- Tactile sensor- Proximity and range sensors- Sensing joint forces- Robotic mission systems- Image gripping- image processing and image segmentation- Pattern recognition, training of vision system.

ROBOTIC CELL DESIGN AND APPLICATION **9 Hours**

Robot work cell design and control- Safety in Robotics- Robot cell layouts- Multiple Robots and machine interference- Robot cycle time analysis- Industrial applications of robots.

ROBOT PROGRAMMING **9 Hours**

Artificial Intelligence and expert systems- Methods of Robot programming- Characteristics of task level languages-Lead through programming methods- Motion interpolation- Artificial Intelligence-Basics- Goals of Artificial intelligence- AI Techniques-Problems-Representation in AI- Problems reduction and solution techniques-Application of AI and KBES in Robots.

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1. C.S.G. Lee, K. S. Fu, and R.C. Gonzalez "Robotics: Control, Sensing, Vision, and Intelligence", McGraw Hill, 2008.
2. Kozyrey, Yu."Industrial Robotics", MIR Publishers, 1985, Mascow.
3. Deb.S.R, "Robotics Technology and Flexible Automation", 2nd Edition, McGraw Hill, 2009.
4. Mikell.P.Groover, Michell Weiss, Roger. N. Nagel, Nicholas G. Odrey and Ashish Dutta, "Industrial Robotics: Technology, Programming and Applications", 2nd Edition, Tata McGraw Hill, 2012.

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5. Timothy Jordanides and Bruce Torby, "Expert Systems and Robotics", Springer - Verlag, 1991, New York.
6. Richard D.Klafter, Thomas A.Chmielewski and Michael Negin, "Robotic Engineering: An Integrated Approach", 1st Edition, Prentice Hall of India, 1989, New Delhi.
7. Low Kin Huat "Industrial Robotics: Programming, Simulation and Applications", 1st Edition, Intech Publishers, 2007.
8. Jesus Aramburo, Antonio R. Trevino "Advances in Robotics, Automation and Control", 1st Edition, Intech Publishers, 2008.

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P15ESTE06	MICRO ELECTRO MECHANICAL SYSTEMS	L	T	P	C
		3	0	0	3

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Apply knowledge of micro fabrication techniques and applications to the design and manufacturing of an MEMS device or a Micro-system.

CO2: Know the major classes, components, and applications of MEMS devices/systems and to demonstrate an understanding of the fundamental principles behind the operation of these devices/systems.

CO3: Summarize the major classes, components, and applications of MEMS devices/systems and to demonstrate an understanding of the fundamental principles behind the operation of these devices/systems.

PRE-REQUISITE

1. NIL

MEMS DEVICES 9 Hours

Piezoresistive pressure sensor- Piezoresistive Accelerometer - Capacitive Pressure Sensor-Accelerometer and Microphone - Resonant Sensor and Vibratory Gyroscope - Micro Mechanical Electric and Optical Switches- Micro Mechanical Motors - Micro Electro Mechanical Systems Analysis and Design of MEMS Devices- MEMS applied to rehabilitation engineering- Nano Sensors.

BASIC MECHANICS OF BEAM AND DIAPHRAGM STRUCTURES 9 Hours

Stress and Strain- Stress and Strain of Beam Structures-Vibration Frequency by Energy Methods Vibration Modes and the Buckling of a Beam- Damped and forced vibration-Basic Mechanics of Diaphragms – Problems.

AIR DAMPING AND ELECTRO STATIC ACTUATION 9 Hours

Drag Effect of a Fluid- Squeeze-film Air Damping-Damping of Perforated Thick Plates-Slide-film Air Damping- Damping in Rarefied –Air Problems- Electro static Forces-Electrostatic Driving of Mechanical Actuator Step and Alternative-Driving –Problems.

CAPACITIVE SENSING AND EFFECTS OF ELECTRICAL EXCITATION 9 Hours

Capacitive Sensing Schemes- Effects of Electrical Excitation: Static Signal- Effects of Electrical Excitation: Step Signal –Effects of Electrical Excitation: Pulse Signal –Problems.

PIEZO RESISTIVE SENSING 9 Hours

Piezoresistive Effect of Silicon-Coordinate Transformation of Second Rank Tensors-Coordinate Transformation of Piezoresistive Coefficient – Piezoresistive Sensing Elements-Polysilicon Piezoresistive Sensing Elements-Analyzing-Piezo resistive Bridge-Problems.

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1. Minhang Bao, **"**Analysis and design principles of MEMS devices", Elsevier Publications, 2005, USA.
2. Nadim Maluf and Kirt Williams, "An Introduction to Micro Electro Mechanical Systems Engineering, Second Edition", Artech House Publishers, June 2004, USA.
3. Gabriel M. Rebeiz , "RF MEMS: Theory, Design, and Technology", 1st Edition, Wiley, 2004, UK.
4. John A. Pelesko and David H. Bernstein, " Modeling MEMS and NEMS", CRC Press, 2002,UK

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P15ESTE07	SYSTEM SIMULATION AND MODELING	L	T	P	C
		3	0	0	3

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Outline the role of modelling and simulation in the systems engineering process.

CO2: Describe key development factors associated with developing complex models and simulations.

CO3: Distinguish different types of models and simulations and the different ways in which they are used.

PRE-REQUISITE

1. Control System

SYSTEM AND SYSTEM ENVIRONMENT 9 Hours

Concept of a system-continuous and discrete systems – models of a system –modeling approaches – advantages and disadvantages of simulation systems-steps in simulation study-point estimates, confidence interval.

PROBABILITY CONCEPTS IN SIMULATION 9 Hours

Random number generation-mid square-mid product method-constant multiplier method-additive congruental method-linear congruential method test for random numbers-the Chi square test – the Kolmogrov- Smimov test – Runs test-Gaps test-Random variable generation – Gaussian, Exponential, Poisson , Uniform, Weibull – Empirical and Normal distribution.

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STATE SPACE BASED MODELS **9 Hours**

Markovian-Non Markovian models – Discrete and Continuous time Markov Chains – Markov reward models – Semi Markov models – Markov regenerative models.

NON STATE SPACE METHODS **9 Hours**

Performance models – queuing models – task precedence graphs – Dependability models – Reliability graphs – Fault tress.

PETRI NET MODEL **9 Hours**

Finite state Automata – Petri nets – Stochastic Petri nets – Stochastic Reward nets – Colored Petri nets – Fluid Petri nets.

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1. Geoffrey Gordon,"Systems Simulation", 2nd Edition, Prentice Hall of India, 1992.
2. Kishore.S.Trivedi, "Probability and Statistics with Reliability, Queuing and Computer Science Applications", 2nd Edition, John Wiley, 2002.
3. Gotrifed B.S.,"Elements of Stochastic Process Simulation", Prentice Hall, 1984.
4. Arson J.S.,Banks J.C., and Nelson B.L., "Discrete Event Systems Simulation", Prentice Hall of India, 1996.
5. Ajmone Marsan M., Kartson DF., Conte G. and Donatelli S., "Modeling with Generalized Stochastic Petri Nets", Willey, New York, 1998.
6. Kleinrock L., "Queueing Systems Theory",Vol.I, Kluwer Academic Press, 1995.

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P15ESTE08 **ADVANCED COMPUTER ARCHITECTURE**

L	T	P	C
3	0	0	3

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: To explain the fundamentals of CPU, Memory and Input, output devices.

CO2: Understand the various techniques to enhance a processors ability to exploit Instruction-level parallelism (ILP), and its challenges.

CO3: Understand multithreading by using ILP and supporting thread-level parallelism (TLP).

PRE-REQUISITE

1. NIL

FUNDAMENTALS OF COMPUTER DESIGN 9 Hours

Review of fundamentals of CPU, Memory and IO – Performance evaluation – Instruction set principles – Design issues – Example Architectures.

INSTRUCTION LEVEL PARALLELISM 9 Hours

Pipelining and handling hazards – Dynamic Scheduling – Dynamic hardware prediction – Multiple issue – Hardware based speculation – Limitations of ILP – Case studies.

INSTRUCTION LEVEL PARALLELISM WITH SOFTWAR APPROACHES 9 Hours

Compiler techniques for exposing ILP – Static branch prediction – VLIW & EPIC – Advanced compiler support – Hardware support for exposing parallelism – Hardware versus software speculation mechanisms – IA 64 and ltanium processor.

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MEMORY AND I/O **9 Hours**

Cache performance – Reducing cache miss penalty and miss rate – Reducing hit time – Main memory and performance – Memory technology. Types of storage devices – Buses – RAID – Reliability, availability and dependability – I/O performance measures – Designing an I/O system.

MULTIPROCESSORS AND THREAD LEVEL PARALLELISM **9 Hours**

Symmetric and distributed shared memory architectures – Performance issues – Synchronization – Models of memory consistency – Multithreading.

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1. John L. Hennessey and David A.Patterson, "Computer Architecture: A Quantitative Approach", 5th Edition, Morgan Kaufmann, 2011.
2. D.Sia, T.Fountain and P.Kacsuk, "Advanced computer Architectures: A Design Space Approach", Addion Wesley, 2009.
3. Hessham EL- Rewini, Mostafa Abd- El – Barr, "Advanced Computer Architecture and Parallel Processing", John Wiley, 2005.
4. Mark D Hill, Norman P Jouppi, Gurindar S Sohi, "Readings in Computer Architecture", Morgan Kaufmann, 2000.
5. Mano.M.M. "Computer System Architecture", Prentice Hall of India, 2009.

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P15ESTE09 **SOFTWARE TECHNOLOGY FOR EMBEDDED SYSTEMS**

L	T	P	C
3	0	0	3

After successful completion of this course, the students should be able to

CO1: Outline the basics and importance of Linker / locator in real-time systems.

CO2: Illustrate the functional requirements of the hardware and software architecture of embedded systems.

CO3: Students familiarize embedded system software & Hardware development tools.

PRE-REQUISITE

1. Real Time Systems
2. Real Time Operating Systems
3. Operating Systems

PROGRAMMING EMBEDDED SYSTEMS **9 Hours**

Embedded Program – Role of Infinite loop – Compiling, Linking and locating – downloading and debugging – Emulators and simulators processor – External peripherals – Toper of memory – Memory testing – Flash Memory.

OPERATING SYSTEM **9 Hours**

Embedded operating system – Real time characteristics – Selection process – Flashing the LED – serial ports – Zilog 85230 serial controlled code efficiency – Code size – Reducing memory usage – Impact of C++.

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HARDWARE FUNDAMENTALS **9 Hours**

Buses – DMA – interrupts – Built-ins on the microprocessor – Conventions used on schematics – Microprocessor Architectures – Software Architectures – RTOS Architectures – Selecting Architecture.

RTOS **9 Hours**

Tasks and Task states – Semaphores – Shared data – Message queues, Mail boxes and pipes – Memory management – Interrupt routines – Encapsulating semaphore and queues – Hard Real-time scheduling – Power saving.

EMBEDDED SOFTWARE DEVELOPMENT TOOLS **9 Hours**

Host and target machines – Linkers / Locators for Embedded Software – Debugging techniques – Instruction set simulators Laboratory tools – Practical example – Source code.

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1. David E.Simon, "An Embedded Software Primer", 1st Edition, Pearson Education, 2004.
2. Michael Bass, "Programming Embedded Systems in C and C++", 1st Edition, O'Reilly, 2003.
3. Raymond J.A.Bhur, Donald L.Bailey, "An Introduction to Real Time Systems", Prentice Hall of India, 2006.
4. Rajkamal, "Embedded system architecture, programming and design", 2nd Edition, Tata McGraw Hill, 2008.
5. Frank Vahid, Tony Givargas, "Embedded System Design - a Unified Hardware / Software Introduction", John Wiley, 2002.

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P15ESTE10 **OPERATING SYSTEMS**

L	T	P	C
3	0	0	3

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Acquire knowledge about the role of various kernel objects used to manage different applications in a multi user, multi-tasking environment.

CO2: Learn the various techniques to achieve synchronization and provide solutions for concurrency issues in real – time system design.

CO3: Outline the disk organization and file system structure, concepts and accessing techniques for virtual memory management in operating systems.

PRE-REQUISITE

1. NIL

INTRODUCTION 9 Hours

Operating System Structure – Operating System Operations – Process Management – Memory Management – Storage Management – Protection and Security – Distributed Systems – Computing Environments – System Structures: Operating System Services – User Operating System Interface – System Calls – Types of System Calls – System Programs – Process Concept: Process Scheduling – Operations on Processes – Inter-process Communication.

MULTITHREADED PROGRAMMING 9 Hours

Overview – Multithreading Models – Threading Issues – Process Scheduling: Basic Concepts – Scheduling Criteria – Scheduling Algorithms – Multiple-Processor Scheduling – Synchronization – The Critical-Section Problem – Peterson's Solution – Synchronization Hardware – Semaphores – Classic problems of Synchronization – Monitors.

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DEADLOCKS **9 Hours**

System Model – Deadlock Characterization – Methods for Handling Deadlocks – Deadlock Prevention – Deadlock Avoidance – Deadlock Detection – Recovery from Deadlock – Memory Management Strategies: Swapping – Contiguous Memory Allocation – Paging – Structure of the Page Table – Segmentation.

VIRTUAL MEMORY MANAGEMENT **9 Hours**

Demand Paging – Copy on Write – Page Replacement – Allocation of Frames – Thrashing – File System: File Concept – Access Methods – Directory Structure – File Sharing – Protection.

IMPLEMENTING FILE SYSTEMS **9 Hours**

File System Structure – File System Implementation – Directory Implementation – Allocation Methods – Free-space Management - Secondary Storage Structure: Disk Structure – Disk Scheduling – Disk Management – Swap-Space Management. Case Study: The Linux System.

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1. Abraham Silberschatz, Peter Baer Galvin and Greg Gagne, "Operating System Principles", 9th Edition, John Wiley & Sons, 2012.
2. Harvey M. Deitel, "Operating Systems", 6th Edition, Pearson Education, 2009.
3. Andrew S. Tanenbaum, "Modern Operating Systems", 4th Edition, Prentice Hall of India, 2014.
4. William Stallings, "Operating System", 8th Edition, Prentice Hall of India, 2014.

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P15ESTE11 ADVANCED EMBEDDED SYSTEMS

L	T	P	C
3	0	0	3

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Summarize the various design phases in system development and the role of communication protocols.

CO2: Outline the RISC features of 32-bit ARM processor working in two different modes and memory management techniques.

CO3: Applies the fundamental knowledge on ARM processor in writing an optimized and effective program by using support tools.

PRE-REQUISITE

1. Embedded System

PRINCIPLES OF EMBEDDED SYSTEM 9 Hours

Introduction - Embedded systems description, definition, design considerations & requirements - Overview of Embedded system Architecture - Categories of Embedded Systems - Product specifications - hardware/software partitioning - iterations and implementation - hardware software integration - product testing techniques. Wired Communication Protocols: UART - Inter Integrated Circuit (I2C)- Serial Peripheral Interface (SPI) - Controller Area Network (CAN).Wireless communication Protocols: Zigbee Protocols – Blue tooth Protocols - IrDA.

ARM PROCESSOR FUNDAMENTALS 9 Hours

ARM core Introduction – Registers – Current Program Status Register – Pipeline –Exception – Interrupts – Vector Table – Core Extension – Architecture Revisions –ARM Processor Families – ARM Instruction Set – Thumb Instruction set – Thumb Register Usuage – ARM – Thumb Interworking – Stack Instruction – Software Interrupt Instruction.

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CACHES AND MMU **9 Hours**

The Memory Hierarchy and Cache Memory – Cache Architecture - Cache Policy –Co Processor and Caches – Flushing and Cleaning Cache Memory – Cache Lockdown – Caches and Software Performance. MMU: Moving from an MPU to an MMU – Virtual Memory – Details of ARM MMU – The Caches and Write Buffer – Co Processor and MMU configuration.

OPTIMIZED PRIMITIVES **9 Hours**

Double Precision Integer Multiplication – Integer Normalization and count Leading Zeros – Division – Square Roots – Transcendental Functions: Log,,exp,sin,cos – Endian Reversal and Bit Operations – Saturated and Rounded Arithmetic – Random Number Generation.

WRITING AND OPTIMIZING ARM ASSEMBLY CODE 9 Hours

Writing Assembly Code – Profiling and Cycle Counting – Instruction Scheduling –Register Allocation – Conditional Execution – Looping Constructs – Bit Manipulation – Efficient Switches – Handling Unaligned Data.

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1. Andrew N.Sloss, Dominic Symes, Chris Wright, "ARM System Developer's Guide (Morgan Kaufmann Series in Computer Architecture and Design)", Morgan Kaufmann, 2004.
2. Tammy Noergaard, "Embedded Systems Architecture", Newnes, 2005.
3. David Seal, "ARM Architecture Reference Manual", 2nd Edition, Addison Wesley, 2005.
4. Steve Furbe, "ARM System-on-Chip Architecture", 2nd Edition, Addison-Wesley Professional, 2000.

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P15ESTE12 **EMBEDDED NETWORKING**

L	T	P	C
3	0	0	3

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: To explain about CAN controller and its features.

CO2: To study about CAN development tools and implementation methods.

CO3: To describe the implementation issues in CAN.

PRE-REQUISITE

1. NIL

EMBEDDED NETWORKING 9 Hours

Embedded networking – code requirements – Communication requirements – Introduction to CAN open – CAN open standard – Object directory – Electronic Data Sheets & Device – Configuration files – Service Data Objectives – Network management CAN open messages – Device profile encoder.

CONTROLLER AREA NETWORKS 9 Hours

CAN open configuration – Evaluating system requirements choosing devices and tools – Configuring single devices – Overall network configuration – Network simulation – Network Commissioning – Advanced features and testing.

CAN CONTROLLER AND DEVELIOPMENT TOOLS 9 Hours

Controller Area Network – Underlying Technology CAN Overview – Selecting a CAN Controller – CAN development tools.

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IMPLEMENTATION OF CAN **9 Hours**

Implementing CAN open Communication layout and requirements – Comparison of implementation methods – Micro CAN open – CAN open source code –Conformance test – Entire design life cycle.

IMPLEMENTATION ISSUES **9 Hours**

Implementation issues – Physical layer – Data types – Object dictionary – Communication object identifiers – Emerging objects – Node states.

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1 Olaf P. Feiffer, Andrew Ayre and Christian Keydel, "Embedded Networking with CAN and CAN open", RTC Books, 2008.
2 Peter Barry and Gerard Hartnett, "Designing Embedded Networking Applications", Intel Press, 2005
3 Gregory J. Pottie and William J. Kaiser, "Principles of Embedded Network System Design", Cambridge University Press, 2009.
4 Jason Andrews, "Co-verification of Hardware and Software for ARM SoC Design (Embedded Technology)", Newnes, 2004.

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P15ESTE13 EMBEDDED SENSOR NETWORKS

L	T	P	C
3	0	0	3

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Learn the various hardware, software platforms that exist for sensor networks.

CO2: Students will learn how to program communicate with embedded system technologies.

CO3: Evaluate the performance of sensor networks.

PRE-REQUISITE

1. NIL

SENSOR NETWORKS 9 Hours

Overview of sensor networks - Constraints and Challenges – Advantages of sensor networks – Applications – Collaborative Processing – Key definitions in sensor networks – Tracking scenario – Problem formulation –Distributed representation and interference of states – Tracking multiple objects – Sensor models – performance comparison and metrics.

NETWORKING SENSORS 9 Hours

Key assumptions – Medium access control – S-MAC Protocol – IEEE 802.15.4 standard and ZigBee – General Issues – Geographic, Energy-Aware Routing – Attribute based routing.

INFRASTRUCTURE ESTABLISHMENT 9 Hours

Topology control – Clustering-Time synchronization – Localization – Task driven sensing- Role of sensor nodes – Information based tasking – Routing and aggregation.

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SENSOR NETWORK DATABASE **9 Hours**

Sensor Database Challenges – Querying the physical environment – Interfaces – In-network aggregation – Data centric storage – Data indices and range queries – Distributed Hierarchical aggregation – Temporal data.

SENSOR NETWORK PLATFORMS AND TOOLS **9 Hours**

Sensor Node Hardware – Sensor network programming challenges – Node level software platforms- Operating system TinyOS – Node level simulators – State centric programming- Applications and future directions.

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1. Feng Zhao, Leonidas Guibas, "Wireless Sensor Networks An information processing approach", Mogan Kanufmann Publishers, 2004
2. Richard Zurawski, "Embedded System Hand Book", CRC Press, 2009.
3. Iran Stojmenovic, "Hand book of sensor networks", John Wiley & Sons, 2005.
4. Michel Banatre, Pedre Jose Marron, Anibal Ollero and Adam Wilisz, "Cooperating Embedded System and Wireless sensor Network", John Willy, 2008.
5. Embedded System Handbook, "Networked Embedded Systems", 2nd Edition, CRC press, 2009.

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P15ESTE14 **EMBEDDED CONTROL OF ELECTRICAL DRIVES**

L	T	P	C
3	0	0	3

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Exposure to fundamentals of microcontroller and able to write simple programs for specific applications.

CO2: List out the techniques for interfacing I/O devices to the microcontroller, including several specific standard I/O devices.

CO3: Comprehend in programming and able to analyze the real time problems.

PRE-REQUISITE

1. Power Electronics

MC68HC11 Microcontroller 9 Hours

Architecture memory organization – Addressing modes – Instruction set – Programming techniques – simple program.

PERIPHERALS OF MC68HC11 9 Hours

I/O ports – handshaking techniques – reset and interrupts – serial communication interface – serial peripheral interface – programmable timer – analog / digital interfacing – cache memory.

8096 ARCHITECTURE 9 Hours

CPU operation – Interrupt structure – Timers – High Speed Input / Output Ports – I/O control and Status registers – Instruction Set – Addressing Modes – Simple Programming – Queues – Tables and Strings – Stack Memories – Key Switch – Parsing.

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PERIPHERALS AND INTERFACING **9 Hours**

Analog Interface – Serial Ports – Watch dog timers – Real Time Clock – Multitasking – Bus Control – Memory Timing – External ROM and RAM expansion – PWM control – A/D interfacing.

CASE STUDY FOR MC68HC118051 AND 8096 **9 Hours**

Real Time clock – DC Motor Speed Control – Generation of Gating Signals for Converters and Inverters – Frequency Measurement – Temperature Control

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1. John B. Peatman, "Design with Micro controllers", McGraw Hill, 2000, Singapore.
2. Michael Slater, "Microprocessor based designs a comprehensive guide to effective Hardware design" Prentice Hall, 2005, New Jersey.
3. Intel Manual on 16 bit embedded controllers, Santa Clara, 2000.
4. Michael khevi, "The M68Hc11 Microcontroller Applications in Control, Instrumentation and Communication", Prentice Hall, 2005, New Jersey.

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P15ESTE15 **DIGITAL IMAGE PROCESSING**

L	T	P	C
3	0	0	3

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Understand the mathematical concepts involved in video processing.

CO2: Analyze the various transformation techniques that can be applied to enhance image quality.

CO3: Apply the knowledge of mathematical technique for real—time video processing.

PRE-REQUISITE

1. NIL

DIGITAL IMAGE FUNDAMENTALS 9 Hours

Image Representation - gray scale and colour Images, image sampling and quantization. Two dimensional orthogonal transforms - DFT, WHT, Haar transform, KLT, DCT- Introduction to transforms on Image and video processing.

IMAGE ENHANCEMENT AND EDGE DETECTION 9 Hours

Image Enhancement - filters in spatial and frequency domains, histogram-based processing, homomorphic filtering. Edge Detection - non parametric and model based approaches, LOG filters, localisation problem- Segmentation -Introduction to Region Growing.

IMAGE RESTORATION 9 Hours

Image Restoration - PSF, circulant and block - circulant matrices, deconvolution, restoration using inverse filtering, Wiener filtering and maximum entropy-based methods.

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MORPHOLOGICAL IMAGE PROCESSING **9 Hours**

Mathematical Morphology - binary morphology, dilation, erosion, opening and closing, duality relations, gray scale morphology, applications such as hit-and-miss transform, thinning and shape decomposition.

IMAGE PROCESSING **9 Hours**

Computer Tomography - parallel beam projection, Radon transform, and its inverse, Back-projection operator, Fourier-slice theorem, CBP and FBP methods, ART, Fan beam projection and applications.

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1. Milian Sonka, Vaclav Hlavac, Roger Boyle, "Image Processing, Analysis and Machine Vision", 3rd Edition, 4th Edition, Cengage Learning, 2014.
2. R.M. Haralick, and L.G. Shapiro, "Computer and Robot Vision", Vol-1, Addison Wesley, 1993.
3. R. Jain, R. Kasturi and B.G. Schunck, "Machine Vision", McGraw Hill, 1995.
4. Kenneth R. Castleman, "Digital Image Processing" Pearson Education, 2008.
5. William. K. Pratt, "Digital Image Processing", John Wiley, 2007, New York.

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P15PETE17 **ADVANCED DIGITAL SIGNAL PROCESSING**

L	T	P	C
3	0	0	3

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Able to understand basics of discrete random signal processing.

CO2: Able to estimate the spectrum and use the filters for noise cancellation and echo cancellation.

CO4: Able to understand concept of multi-rate digital signal processing & wavelet transformer.

PRE-REQUISITE

1. Signals and System
2. Digital Signal Processing

DISCRETE RANDOM SIGNAL PROCESSING 9 Hours

Discrete Random Processes – Ensemble averages, stationary processes, Autocorrelation and Auto covariancematrices – Parseval‟s Theorem – Wiener-Khintchine Relation – Power Spectral Density – Periodogram Spectral Factorization – Filtering random processes – Low Pass Filtering of White Noise – Parameter estimation: Bias and consistency.

SPECTRUM ESTIMATION 11 Hours

Estimation of spectra from finite duration signals – Non- Parametric Methods – Correlation Method – Periodogram Estimator – Performance Analysis of Estimators – Unbiased, Consistent Estimators – Modified periodogram – Bartlett and Welch methods – Blackman – Tukey method - Parametric Methods – AR, MA, and ARMA model based spectral estimation – Parameter Estimation –Yule-Walker equations – Solutions using Durbin‟s algorithm.

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LINEAR ESTIMATION AND PREDICTION **8 Hours**

Linear prediction – Forward and backward predictions – Solutions of the Normal equations – Levinson - Durbin algorithms – Least mean squared error criterion – Wiener filter for filtering and prediction – FIR Wiener filter and Wiener IIR filters – Discrete Kalman filter.

ADAPTIVE FILTERS **8 Hours**

FIR adaptive filters – Adaptive filter based on steepest descent method – Widrow-Hoff LMS adaptive algorithm – Normalized LMS – Adaptive channel equalization – Adaptive echo cancellation – Adaptive noise cancellation – Adaptive recursive filters (IIR) – RLS adaptive filters – Exponentially weighted RLS – Sliding window RLS.

MULTIRATE DIGITAL SIGNAL PROCESSING **9 Hours**

Mathematical description of change of sampling rate – Interpolation and Decimation – Decimation by an integer factor – Interpolation by an integer factor – Sampling rate conversion by a rational factor – Filter implementation for sampling rate conversion – direct form FIR structures – Polyphase filter structures – Timevariant structures – Multistage implementation of multirate system – Application to sub band coding – Wavelet transform and filter bank implementation of wavelet expansion of signals.

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1. Monson H. Hayes, "Statistical Digital Signal Processing and Modeling", Wiley India, 2008.
2. John G. Proakis and Dimitris G. Manolakis, "Digital Signal Processing", 4th Edition, Prentice Hall of India, 2006, New Delhi.
3. John G. Proakis, Charles M. Rader, "Algorithms for Statistical Signal Processing", Pearson Education, 2002, New Delhi.

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P15ESTE16 DSP INTEGRATED CIRCUITS

L	T	P	C
3	0	0	3

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Gain knowledge of design methodologies and techniques applicable to VLSI technology.

CO2: Design various filter circuit and analyze the problem of word length effect.

CO3: Learn the fundamentals of the arithmetic units in DSP processor.

PRE-REQUISITE

1. Digital Signal Processing

DSP INTEGRATED CIRCUITS AND VLSI CIRCUIT TECHNOLOGIES 9 Hours

Standard digital signal processors-Application specific IC's for DSP-DSP systems-DSP system design- Integrated circuit design-MOS transistors-MOS logic-VLSI process technologies-Trends in CMOS technologies.

DIGITAL SIGNAL PROCESSING 9 Hours

Digital signal processing-Sampling of analog signals-Selection of sample frequency-Signal processing systems-Frequency response - Transfer functions - Signal flow graphs- Filter structures- Adaptive DSP algorithms -DFT-The Discrete Fourier Transform - FFT-The Fast Fourier Transform Algorithm - Image coding - Discrete cosine transforms.

DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS 9 Hours

FIR filters - FIR filter structures- FIR chips - IIR filters - Specifications of IIR filters - Mapping of analog transfer functions - Mapping of analog filter structures - Multirate systems - Interpolation with an integer factor L - Sampling rate change with a ratio L/M - Multirate filters - Finite word

length effects -Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

DSP ARCHITECTURES AND SYNTHESIS OF DSP ARCHITECTURES **9 Hours**

DSP system architectures - Standard DSP architecture - Ideal DSP architectures - Multiprocessors and multicomputer - Systolic and Wave front arrays - Shared memory architectures. Mapping of DSP algorithms onto hardware - Implementation based on complex PEs - Shared memory architecture with Bit – serial PEs.

ARITHMETIC UNITS AND INTEGRATED CIRCUIT DESIGN **9 Hours**

Conventional number system - Redundant Number system, Residue Number System. Bit-parallel and Bit-Serial arithmetic, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Layout of VLSI circuits, FFT processor, DCT processor and Interpolator as case studies.

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1. Lars Wanhammer, "DSP Integrated Circuits", 1st Edition, Academic Press, 1999, New York.
2. Robert J. Schilling, "Fundamentals of Digital Signal Processing using MATLAB", 2nd Edition, Pearson Education, 2010.
3. A.V.Oppenheim et.al, "Discrete-time Signal Processing", 3rd Edition, Pearson Education, 2009.
4. Emmanuel C. Ifeachor, Barrie W. Jervis, "Digital signal processing – A practical approach", 2nd Edition, Pearson Education, 2001.
5. Keshab K.Parhi, "VLSI digital Signal Processing Systems design and Implementation", 1st Edition, Wiley India, 2010.

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P15ESTE17	EMBEDDED COMMUNICATION SOFTWARE DESIGN	L	T	P	C
		3	0	0	3

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Explain the OSI reference model and communication layer.

CO2: Describe the procedure software partitioning and speed up the communication process.

CO3: Distinguish the various management schemes and describe Multi board communication.

PRE-REQUISITE

1. NIL

OSI REFERENCE MODEL 9 Hours

OSI Reference Model – Communication Devices – Communication Echo System – Design Consideration – Host Based Communication – Embedded Communication System – OS Vs RTOS.

SOFTWARE PARTITIONING 9 Hours

Software Partitioning – Limitation of strict Layering – Tasks & Modules – Modules and Task Decomposition – Switch - Bridges - Routers – Protocol Implementation: STP - RSTP – Management Types (SNMP) – Debugging Protocols.

DATA STRUCTURES 9 Hours

Tables & other Data Structures – Partitioning of Structures and Tables – Implementation – Speeding Up access – Table Resizing – Table access routines – Buffer and Timer Management – Third Party Protocol Libraries.

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MANAGEMENT SCHEMES **9 Hours**

Management Software – Device Management – Management Schemes – Router Management – Management of Sub System Architecture – Device to manage configuration – System Start up and configuration.

MULTI BOARD COMMUNICATION **9 Hours**

Multi Board Communication Software Design – Multi Board Architecture – Single control Card and Multiple line Card Architecture – Interface for Multi Board software – Failures and Fault – Tolerance in Multi Board Systems – Hardware independent development – Using a COTS Board – Development Environment – Test Tools.

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1. Sridhar .T, "Designing Embedded Communication Software", CMP Books, 2003.
2. Ahmed Amine Jerraya, Sungjoo Yoo, Diederix Veskest and Norbest Whn, "Embedded Software for SOC", 1st Edition, Kulwar Academic Publishers, 2004.
3. Comer. D, "Computer networks and Internet", 3rd Edition, Prentice Hall, 2001.

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P15ESTE18	DATA COMMUNICATION AND NETWORKS	L	T	P	C
		3	0	0	3

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Describe the various components of Network.

CO2: Outline the various OSI layers.

CO3: Distinguish the various application protocol.

PRE-REQUISITE

1. NIL

INTRODUCTION TO NETWORK COMPONENTS 9 Hours

Components of network – Topologies – WAN / LAN – OSI – ISO layered Architecture – digital Modulation and demodulation techniques – Bit error rates – Line coding – Error correcting codes.

DATA LINK LAYER 9 Hours

Design issues – CRC technique and sliding window techniques – Performance analysis of sliding window techniques – Framing formats – Case Study – HDLC protocols – Medium access control – CSMA / CD – Token ring and token bus – FDDI – Wireless LAN – Performance analysis of MAC protocols – Bridges.

NETWORK LAYER 9 Hours

Circuit switching – packet switching – Design issues – IP addressing and IP datagram – Routers and gateways – Routing –Subnetting – CIDR – ICMP – ARP – RARP – basics of Ipv6 – QoS.

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TRANSPORT LAYER **9 Hours**

TCP and UDP – Error handling and flow control – Congestion control – TCP Retransmission – Timeout – Socket Abstraction.

APPLICATION SERVICES **9 Hours**

Simple Mail Transfer Protocol (SMTP) – Secure File Transfer Protocols (SFTP), telnet, the World Wide Web (WWW) - Hypertext Transfer Protocol (HTTP) - Domain name service (DNS), Security, and Multimedia applications - DHCP.

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1. William Stallings, "Data and Computer Communications", 8th Edition, Prentice Hall, 2003.
2. Larry Peterson, Bruce S Davie "Computer Networks: A Systems Approach", 5th Edition, Morgan Kaufmann Publishers, 1999.
3. James F Kurose, "Computer Networking: A Top – Down Approach Featuring the Internet", 6th Edition, Addison Wesley, 2002.
4. W.Richard Stevens and Gary R Wright, "TCP / IP Illustrated", Addison Wesley, Volume 1 & 2, 2001.
5. Douglas E Corner, "Internetworking with TCP / IP", Volume 1 & 2, 2000.

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P15ESTE19	WIRELESS AND MOBILE COMMUNICATION	L	T	P	C
		3	0	0	3

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: To study the technologies used in wireless communication and overall GSM cellular concept.

CO2: To understand the various wireless networks.

CO3: To study the different diversity techniques.

PRE-REQUISITE

1. NIL

INTRODUCTION TO WIRELESS COMMUNICATION 9 Hours

Wireless Transmission-signal propagation-spread spectrum-Satellite Networks- Capacity Allocation-FAMA-DAMA-MAC.

MOBILE NETWORKS 9 Hours

Cellular Wireless Networks-GSM-Architecture-Protocols-Connection Establishment - Frequency Allocation-Routing-Handover-Security-GPRS.

WIRELESS NETWORKS 9 Hours

Wireless LAN-IEEE 802.11 Standard-Architecture-Services-Architecture of Ad. Hoc Network - HiperLan-Blue Tooth technology and its applications.

ROUTING 9 Hours

Mobile IP-DHCP- AdHoc Networks-Proactive and Reactive Routing Protocols with applications- features- Multicast Routing algorithms.

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TRANSPORT AND APPLICATION LAYERS **9 Hours**

TCP over Adhoc Networks-WAP-Architecture-WWW Programming Model-WDP - WTLS-WTP-WSP-WAE-WTA Architecture-WML-WML scripts.

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1 Kaveh Pahlavan, Prasanth Krishnamoorthy, "Principles of Wireless Networks", Prentice Hall of India, 2003

2 Uwe Hansmann, Lothar Merk, Martin S. Nicklons and Thomas Stober, "Principles of Mobile computing", Springer, 2003, New York.

3 C.K.Toh, "AdHoc mobile wireless networks", Prentice Hall, 2007.

4 Charles E. Perkins, "Adhoc Networking", Addison-Wesley, 2001.

5 Jochen Schiller, "Mobile communications", 2nd Edition, PHI/Pearson Education, 2003.

6 William Stallings, "Wireless communications and Networks", PHI/Pearson Education, 2009.

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P15ESTE20	VLSI ARCHITECTURE AND DESIGN METHODOLOGIES	L	T	P	C
		3	0	0	3

COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Acquire the concept of VLSI design methodologies and hazards in digital circuit.

CO2: Realize the architecture of programmable ASIC and realization of high speed VLSI circuits.

CO3: Acquire the concept of simulation, synthesis and testing of digital circuits.

PRE-REQUISITE

1. FPGA Architecture

VLSI DESIGN METHODOLOGIES 9 Hours

Overview of digital VLSI design methodologies – Trends in IC Technology – Advanced Boolean algebra – Shannon's expansion theorem – Consensus theorem – Octal designation- Run measure – Buffer gates - Gate expander – Reed Muller expansion – Synthesis of multiple output combinational logic circuits by product map method – Design of static hazard free, dynamic hazard free logic circuits.

ANALOG VLSI AND HIGH SPEED VLSI 9 Hours

Introduction to analog VLSI – realization of neural networks and switched capacitor filters – Sub-micron technology and Gas VLSI Technology.

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PROGRAMMABLE ASICS **9 Hours**

Anti fuse – static RAM – EPROM and technology – PREP bench marks – Actel ACT – Xilinx LCA – Altera flex – Altera MAX DC & AC inputs and outputs – Clock and power inputs – Xilinx I/O blocks.

PROGRAMMABLE ASIC DESIGN SOFTWARE **9 Hours**

Actel ACT – Xilinx LCA – Xilinx CPLD – Altera MAX 5000 and 7000 – Altera MAX 9000 – design systems – logic synthesis – half gate – schematic entry – Low level design language – PLA tools – EDIF – CFI design representation.

LOGIC SYNTHESIS, SIMULATION AND TESTING **9 Hours**

Basic features of VHDL language for behavioral modeling and simulation – Summary of VHDL data types – Dataflow and structural modeling – VHDL and logic synthesis – Circuit and layout verification – Types of simulation – Boundary scan test – Fault simulation – Automatic test pattern generation – design examples.

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1. William I.Fletcher, "An Engineering Approach to Digital Design", Prentice Hall of India, 1997.
2. Amar Mukharjee, "Introduction to NMOS and CMOS VLSI System Design", Prentice Hall, 1986.
3. M.J.S. Smith, "Application – specific integrates circuits", Addison Wesley Longman Inc. 1997.
4. Frederick J.Hill and Gerald R.Peterson, "Computer Aided Logical Design with emphasis on VLSI", 4th Edition, Wiley, 1993.

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P15ESTE21 **VLSI DESIGN**

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COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Acquire the depth of concepts in fabrication techniques in CMOS.

CO2: Acquire the electrical properties of CMOS and layout design rules.

CO3: Realize the testing of VLSI circuits and logic design of digital circuits.

PRE-REQUISITE

1. Digital Design

VLSI DESIGN METHODOLOGY & MOS TECHNOLOGY 9 Hours

VLSI Design process — Architectural Design — Logical design — Physical design — Layout styles — Full custom — Semicustom approaches - An overview of wafer fabrication — Wafer processing — Oxidation — Patterning — Diffusion — Ion implantation — Deposition — Silicon gate NMOS process — CMOS processes — nWell — pWell — Twintub — Silicon on insulator.

ELECTRICAL PROPERTIES OF MOS AND CMOS CIRUITS 9 Hours

MOS enhancement transistor — PMOS enhancement transistor — Threshold voltage — Threshold voltage equations — MOS device equations — Basic DC equations — Second order effects — MOS modules — Small signal AC characteristics — NMOS inverter— Steered Input to an NMOS inverter — Depletion mode and enhancement mode pull-ups — CMOS inverter — DC characteristics — Inverter delay —

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Pass transistor — Transmission gate.

MOS AND CMOS CIRCUIT DESIGN PROCESSES 9 Hours

CMOS process enhancements — Interconnect - Circuit elements - Latch up – Latch up prevention techniques - Need for Layout design rules — Mead conway design rules for the silicon gate NMOS process — CMOS nWell pWell design rules — Simple Layout examples — Sheet resistance — Area capacitance — Wiring Capacitance — Drive large capacitive loads.

LOGIC DESIGN 9 Hours

Switch Logic — Pass Transistor and transmission gate — Gate Logic — Inverter — Two input NAND gate — NOR gate — Other forms of CMOS logic — Dynamic CMOS logic — Clocked CMOS logic — Precharged domino CMOS logic — Structured design — Simple combinational logic design examples — Parity generator — Multiplexers — locked sequential circuits —Two phase clocking — Charge storage — Dynamic register element — NMOS and CMOS — Dynamic shift register — Semi static register — JK flip flop circuit.

TESTING 9 Hours

Importance of testing – Boundary – Scan Test – faults – fault simulation – Automatic Test – Pattern Generation – IDDQ Test – Built in Self Test – A simple test example.

Theory:45 Hrs Total: 45 Hrs

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REFERENCES

1. Douglas A. Pucknell, K. Eshragian, "Basic VLSI Design", 3rd Edition, Prentice Hall of India, 2009, New Delhi.
2. Neil. H.E.Weste, Kamaran Eshraghian, "Principles of CMOS VLSI Design", 2nd Edition, Addison Wesley Publications, 2005.
3. Amar Mukherjee, "Introduction to NMOS and CMOS VLSI system design", 2nd Edition, Prentice Hall, 2002.
4. Wayne Wolf, "Modern VLSI Design: Systems on Si1icon", 3rd Edition, Pearson Education, 2002.
5. Eugene D.Fabricius, "Introduction to VLSI Design", 1st Edition, Tata McGraw Hill, 1990, New Delhi.

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P15ESTE22 **ASIC AND FPGA DESIGN**

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COURSE OUTCOMES

After successful completion of this course, the students should be able to

CO1: Acquire the concepts of CMOS and ASIC library and I/O cells.
CO2: Know the internal architecture of ASIC family.
CO3: Acquire the knowledge of floor planning, placement, routing and HDL synthesis.

PRE-REQUISITE

1. NIL

INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN — 9 Hours

Types of ASICs – Design Flow – CMOS transistors, CMOS design rules – Combinational Logic Cell – Sequential logic cell – Data path logic cell – Transistors as Resistors –Transistor Parasitic Capacitance – Logical effort – Library cell design – Library architecture.

PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMBALE ASIC I/O CELLS — 9 Hours

Anti fuse – static RAM – EPROM and EEPROM technology – PREP bench marks –Actel ACT – Xilinx LCA – Altera FLEX – Altera MAX DC & AC inputs and outputs –Clock and power inputs – Xilinx I/O blocks.

PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY — 9 Hours

Actel ACT – Xilinx LCA – Xilinx EPLD – Altera MAX 5000 and 7000 –

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Altera MAX 9000 Altera FLEX – Design systems – Logic Synthesis – Half Gate ASIC – Schematic entry – Low level design language – PLA tools – EDIF – CFI design representation.

LOGIC SYNTHESIS, SIMULATION AND TESTING **9 Hours**

Verilog and logic synthesis – VHDL and logic synthesis - Types of simulation – Boundary scan test – Fault simulation – Automatic test pattern generation.

ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING **9 Hours**

System partition – FPGA partitioning – partitioning methods – floor planning – placement – physical design flow – global routing – detailed routing – special routing – circuit extraction – DRC.

Theory:45 Hrs **Total: 45 Hrs**

REFERENCES

1. M.J.S. SMITH, "Application – Specific Integrated Circuits", 1st Edition, Addison Wesley, 2003.
2. Andrew Brown, "VLSI Circuits and Systems in Silicon", McGraw Hill, 1991.
3. S.D.Brown, R.J.Francis, J.Rox, Z.G.Uranesic, "Field Programmable Gate Arrays", Kluever Academic Publishers, 1992.
4. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing", McGraw Hill, 1994.
5. S.Y. Kung, H.J.Whilo House, T.Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1985.
6. Jose E.France, Yannis Tsividis, "Design of Analog – Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994

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ONE CREDIT COURSES

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P15ESIN01 **Internet of Things**

Introduction – Concepts behind the Internet of Things. - The IoT paradigm - Smart objects - Bits and atoms - Goal orientation - Convergence of technologies

Technologies behind the Internet of Things. - RFID + NFC - Wireless networks + WSN - RTLS + GPS - Agents + Multiagent systems

Theory:15 Hrs **Total: 15 Hrs**

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P15ESIN02 EMBEDDED SYSTEM IN CARS

Traction control system – Cruise control system – electronic control of automatic transmission –antilock braking system –electronic suspension system – working of airbag and role of MEMS in airbag systems – centralized door locking system –climate control of cars.

Theory:15 Hrs **Total: 15 Hrs**

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P15ESIN03

ADVANCED COMMUNICATION PROTOCOLS

Basic need of communication protocols - I2C protocol – RS232 protocol – GSM/CDMA - wireless protocols – programs - 3G network.

Theory:15 Hrs **Total: 15 Hrs**

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P15ESIN04 PLC Based Automation in Industries

Module I

Introduction to Programmable Logic Controller PLC evolution – hardwire control system compared with PLC system - advantages of PLCs – criteria for selection of suitable PLC - Block diagram of PLC – principle of operation – CPU – memory organization – I/O modules – Input types – Logic, Analog – pulse train – expansion modules – power supplies to PLC – modular PLCs - list of various PLCs available

Module II

Input and Output Modules Input Modules Discrete input module – AC input module – DC input module – sinking and sourcing – sensor input – special input modules – Sensors – limit switch, reed switch, photo electric sensor, inductive proximity sensor – Input Addressing scheme in important commercial PLCs. Output modules Discrete output module – TTL output module – Relay output – Isolated output module – surge suppression in output – Analog outputs – open collector output. Output Addressing scheme in important commercial PLCs.

Theory:15 Hrs **Total: 15 Hrs**

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