KUMARAGURU COLLEGE OF TECHNOLOGY, COIMBATORE-49
(An Autonomous Institution Affiliated to Anna University, Chennai)

CURRICULUM 2013

M.E – EMBEDDED SYSTEM

SEMESTER – I

S. No	Code No	Course Title	L	T	P	C
Theory						
1.	P13MAT106	Applied Mathematics for Embedded Systems	3	1	0	4
2.	P13EST101	Advanced Digital System Design	3	0	0	3
3.	P13EST102	Embedded Systems Design	3	0	0	3
4.	P13EST103	Real Time Systems	3	0	0	3
5.	P13ESTE**	Elective - I	3	0	0	3
6.	P13ESTE**	Elective - II	3	0	0	3
Practical						
1.	P13ESP101	Embedded System Laboratory I	0	0	3	1

TOTAL PERIODS – 22 **TOTAL CREDITS – 20**

SEMESTER – II

S. No	Code No	Course Title	L	T	P	C
Theory						
1.	P13EST201	Real Time Operating Systems	3	0	0	3
2.	P13EST202	Embedded Control Systems	3	0	0	3
3.	P13EST203	Advanced Optimisation Techniques	3	0	0	3
4.	P13EST204	VLSI Architecture and Design Methodologies	3	0	0	3
5.	P13ESTE**	Elective - III	3	0	0	3
6.	P13ESTE**	Elective - IV	3	0	0	3
Practical						
1.	P13ESP201	Embedded System Laboratory II	0	0	3	1

TOTAL PERIODS – 21 **TOTAL CREDITS - 19**

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SEMESTER – III

S. No	Code No	Course Title	L	T	P	C
Theory						
1	P13ESTE**	Elective - V	3	0	0	3
2	P13ESTE**	Elective - VI	3	0	0	3
3	P13ESTE**	Elective - VII	3	0	0	3
Practical						
1	P13ESP301	Embedded System Laboratory III	0	0	3	1
2	P13ESP302	Project (Phase-I)	0	0	12	6

TOTAL PERIODS – 24 **TOTAL CREDITS – 16**

SEMESTER – IV

S. No	Code No	Course Title	L	T	P	C
Practical						
1	P13ESP401	Project - (Phase II)	0	0	24	12

TOTAL PERIODS – 24 **TOTAL CREDITS** – 12

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LIST OF ELECTIVE

S. No	Code No	Course Title	L	T	P	C
1	P13ESTE01	Intelligent Control	3	0	0	3
2	P13ESTE02	Advanced Digital Signal Processing	3	0	0	3
3	P13ESTE03	VHDL	3	0	0	3
4	P13ESTE04	VLSI Design	3	0	0	3
5	P13ESTE05	Advanced Embedded Systems	3	0	0	3
6	P13ESTE06	Software Technology for Embedded Systems	3	0	0	3
7	P13ESTE07	Embedded Sensor Networks	3	0	0	3
8	P13ESTE08	Embedded Processors	3	0	0	3
9	P13ESTE09	Embedded Networking	3	0	0	3
10	P13ESTE10	Micro Electro Mechanical Systems	3	0	0	3
11	P13ESTE11	ASIC Design	3	0	0	3
12	P13ESTE12	System Simulation and Modelling	3	0	0	3
13	P13ESTE13	Digital Image Processing	3	0	0	3
14	P13ESTE14	Industrial Automation And Control	3	0	0	3
15	P13ESTE15	Advanced Computer Architecture	3	0	0	3
16	P13ESTE16	Digital Control Systems	3	0	0	3
17	P13ESTE17	Operating Systems	3	0	0	3
18	P13ESTE18	Embedded Communication software design	3	0	0	3
19	P13ESTE19	DSP Integrated Circuits	3	0	0	3
20	P13ESTE20	Industrial Robotics and Expert Systems	3	0	0	3
21	P13ESTE21	Data Communication and Networks	3	0	0	3
22	P13ESTE22	Embedded Control of Electrical Drives	3	0	0	3
23	P13ESTE23	Micro controller Based System Design	3	0	0	3
24	P13ESTE24	Wireless and Mobile Communication	3	0	0	3
25	P13ESTE25	DSP For Embedded System	3	1	0	4
26	P13ESTE26	Solid State Converters	3	0	0	3

* - P13ESTE01
** - P13ESTE02
*** - P13ESTE03
**** - P13ESTE04

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P13MAT106	APPLIED MATHEMATICS FOR EMBEDDED SYSTEMS	L T P C 3 1 0 4

On completion of the course, the students are expected

- to solve initial and boundary value problems on applying Laplace transform.
- to acquire knowledge in the solution of Bessel functions and Legendre polynomials.
- to acquire knowledge in the concepts of Fourier analysis and Z-transforms.
- to acquire knowledge in probability, random variables and standard distributions
- to deal the problems under queuing theory.

UNIT I THE WAVE EQUATION 9

Solution of initial and boundary value problems – Characteristics – D'Alembert's Solution – Significance of Characteristic curves – Laplace transform solutions for displacement in a long string – a long string under its weight – a bar with prescribed force on one end – free vibration of a string.

UNIT II SPECIAL FUNCTIONS 9

Series solutions – Bessel's equation – Bessel Functions – Legendre's equation – Legendre Polynomials – Rodrigue's formula – Recurrence relations – Generating Functions and orthogonal property for Bessel functions of the first kind – Legendre Polynomials.

UNIT III FOURIER ANALYSIS AND Z –TRANSFORMS 9

Discrete Fourier Transforms and its properties – Fourier series and its properties – Fourier representation of finite duration sequences – Z-transform – Properties of the region of convergence – Inverse Z-transform – Z-transform properties.

UNIT IV PROBABILITY AND RANDOM VARIABLES 9

Probability – Random variables – Binomial, Poisson, Geometric, Uniform, Normal, Exponential distributions – Moment generating functions and their properties – Functions of Random variables.

UNIT V QUEUING THEORY 9

Queuing characteristics, single server and parallel server models:
(M / M / 1): $(\infty / FIFO)$, (M / M / k): $(\infty / FIFO)$, (M / M / 1): $(N / FIFO)$, (M / M / k): $(N / FIFO)$ M/G/1 queuing system – P-K formula

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L = 45 T = 15 Total = 60 Periods

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REFERENCES

1. Andrews L.C., and Shivamoggi, B.K. Integral Transforms for Engineers, Prentice Hall of India Pvt. Ltd, New Delhi, 2003.
2. Gupta, S.C and Kapoor V.K., Fundamentals of Mathematical Statistics, Sultan Chand and sons, New Delhi, 2001.
3. Taha H .A., Operations Research: An Introduction, Pearson Education Edition, Asia, New Delhi, Seventh Edition 2002.
4. O'Neil P.V., Advanced Engineering Mathematics, Thomson Brooks/Cole, Singapore, 5th Edition, 2003.
5. Andrews L.C., Special Functions of Mathematics for Engineers, McGraw Hill, Inc., Singapore, 2nd Edition, 1992.

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P13EST101 ADVANCED DIGITAL SYSTEM DESIGN

L	T	P	C
3	0	0	3

UNIT I SEQUENTIAL CIRCUIT DESIGN 9

Analysis of Clocked Synchronous Sequential Networks (CSSN) Modeling of CSSN – State Stable Assignment and Reduction – Design of CSSN – Design of Iterative Circuits – ASM Chart – ASM Realization.

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9

Analysis of Asynchronous Sequential Circuit (ASC) – Flow Table Reduction – Races in ASC – State Assignment – Problem and the Transition Table – Design of ASC – Static and Dynamic Hazards – Essential Hazards – Data Synchronizers – Designing Vending Machine Controller – Mixed Operating Mode Asynchronous Circuits.

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9

Fault Table Method – Path Sensitization Method – Boolean Difference Method – Kohavi Algorithm – Tolerance Techniques – The Compact Algorithm – Practical PLA's – Fault in PLA – Test Generation – Masking Cycle – DFT Schemes – Built-in Self Test.

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9

EPROM to Realize a Sequential Circuit – Programmable Logic Devices – Designing a Synchronous Sequential Circuit using a GAL – EPROM – Realization State machine using PLD – FPGA – Xilinx FPGA – Xilinx 2000 - Xilinx 3000

UNIT V SYSTEM DESIGN USING VHDL 9

VHDL Description of Combinational Circuits – Arrays – VHDL Operators – Compilation and Simulation of VHDL Code – Modelling using VHDL – Flip Flops – Registers – Counters – Sequential Machine – Combinational Logic Circuits - VHDL Code for – Serial Adder, Binary Multiplier – Binary Divider – complete Sequential Systems – Design of a Simple Microprocessor.

L: 45 Total: 45 Hrs

REFERENCES:

1. Donald G. Givone "Digital principles and Design" Tata McGraw Hill 2002.
2. Charles H. Roth Jr. "Digital System Design using VHDL" Thomson Learning, 1998.
3. Navabi.Z. "VHDL Analysis and Modeling of Digital Systems. McGraw International, 1998.
4. Parag K Lala, "Digital System design using PLD" BS Publications, 2003
5. Skahill. K, "VHDL for Programmable Logic" Pearson education, 1996.

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P13EST102 EMBEDDED SYSTEMS DESIGN

L	T	P	C
3	0	0	3

UNIT I EMBEDDED SYSTEM DESIGN 9

Embedded systems descriptions & definitions – Challenges - Embedded system design considerations and requirements, processor selection and tradeoffs. - Overview of board development process - Configurable/Reconfigure Embedded Systems.- Hardware /Software co verification-Microprocessor/microcontroller

UNIT II DESIGN USING PIC MICROCONTROLLER 9

CPU Architecture and instruction set – Program and Data memory – CPU registers – IO port expansion – External Interrupts and Timers – RB0/INT – Timer0 – Compare and Capture mode – Timer 1 – PWM outputs – I2C operation – ADC – UART.

UNIT III EMBEDDED COMPUTING PLATFORM 9

CPU bus- Memory devices- I/O devices- Component interfacing- Designing with Microprocessors- Development and Debugging- Design example- Design patterns- Dataflow graphs- Assembly and Linking- Basic compilation techniques- Analysis and Optimization

UNIT IV DISTRIBUTED EMBEDDED SYSTEM DESIGN 9

Inter-process communication- Signals – Shared memory Communication- Accelerated design- Design for video accelerator- Networks for embedded systems- Networks based design- Internet enabled systems. Embedded Design methodologies and tools – design flows – designing hardware and software components - requirement analysis and specification

UNIT V SOFTWARE DEVELOPMENT AND TOOLS 9

Embedded system evolution trends. Round - Robin, robin with Interrupts, function-One-Scheduling Architecture, Algorithms. Introduction to-assembler-compiler-cross compilers and Integrated Development Environment (IDE). Object Oriented Interfacing, Recursion, Debugging strategies, Simulators-Logic Analyzers - ICD and ICE. (MPLAB IDE Programming)

L: 45 Total: 45 Hrs

REFERENCES

1. Raymond J.A.Bhur and Donald L.Bialey, "An Introduction to Real Time Systems: From Design to Networking with C/C++", Prentice Hall Inc., New Jersey, 1999.
2. Wayne Wolf, "Computers as Components: Principles of Embedded Computer Systems Design", Morgan Kaufman Publishers, 2004.
3. David E Simon, "An embedded software primer ", Pearson education Asia, 2001
4. John B. Peatman," Design with PIC microcontrollers", Pearson Education Singapore - 1998.
5. Tim Wilmshurst ," Designing Embedded Systems with PIC Microcontrollers: Principles and Applications**"** Newness Publisher- 2007

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P13EST103 **REAL TIME SYSTEMS**

L	T	P	C
3	0	0	3

UNIT I REAL TIME SYSTEMS 9

Introduction – Issues in Real Time Computing, Structure of a Real Time System, Task classes, Performance Measures for Real Time Systems, Estimating Program Run Times. Task Assignment and Scheduling – Classical uniprocessor scheduling algorithms, Uniprocessor scheduling of IRIS tasks, Task assignment, Mode changes, and Fault Tolerant Scheduling.

UNIT II PROGRAMMING LANGUAGES AND TOOLS 9

Programming Languages and Tools – Desired language characteristics, Data typing, Control structures, Facilitating Hierarchical Decomposition, Packages, Run – time (Exception) Error handling, Overloading and Generics, Multitasking, Low level programming, Task Scheduling, Timing Specifications, Programming Environments, Run – time support.

UNIT III REAL TIME DATABASES 9

Real time Databases – Basic Definition, Real time Vs General Purpose Databases, Main Memory Databases, Transaction priorities, Transaction Aborts, Concurrency control issues, Disk Scheduling Algorithms, Two – phase Approach to improve Predictability, Maintaining Serialization Consistency, Databases for Hard Real Time Systems.

UNIT IV COMMUNICATION 9

Real – Time Communication – Communications media, Network Topologies Protocols, Fault Tolerant Routing. Fault Tolerance Techniques – Fault Types, Fault Detection. Fault Error containment Redundancy, Data Diversity, Reversal Checks, Integrated Failure handling.

UNIT V EVALUATION TECHNIQUES 9

Reliability Evaluation Techniques – Obtaining parameter values, Reliability models for Hardware Redundancy, Software error models. Clock Synchronization – Clock, A Nonfault – Tolerant Synchronization Algorithm, Impact of faults, Fault Tolerant Synchronization in Hardware, Fault Tolerant Synchronization in software.

L: 45 Total: 45 Hrs

REFERENCES

1. C.M. Krishna, Kang G. Shin, "Real – Time Systems", McGraw – Hill International Editions, 2005.
2. Stuart Bennett, "Real Time Computer Control – An Introduction", Prentice Hall of India, 2000.
3. Peter D.Lawrence, "Real Time Micro Computer System Design – An Introduction", McGraw Hill, 1988.
4. S.T. Allworth and R.N.Zobel, "Introduction to real time software design", Macmillan, 2nd Edition, 2005.
5. R.J.A Buhur, D.L Bailey, "An Introduction to Real – Time Systems", Prentice – Hall International, 2002.

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P13ESP101	EMBEDDED SYSTEM LABORATORY I	L	T	P	C
		0	0	3	1

LIST OF EXPERIMENTS:

8051 Micro controller

IO Programming

1. Read data from port P2 and P3. Add data and display result on port P0. Glow LED connected at port pinP1.1 if carry flag set after addition.
2. Read data from port P2 and P3. Multiply data and display result on port P0 and P1
3. Write program to read switch connected at port pin P1.0, toggle it and send to port pin P1.1
4. Write a program to generate square wave of 50% duty cycle having frequency 5 KHz at port pin P1.0 using timer 1 in mode 2. Modify program to generate pulse waveform of 70% duty cycle using timer on the same pin.

Interrupts and Timer application

5. Generate external interrupt INT0 and INT1 by connecting push button switch. Glow LEDs connected at port 1 one by one when interrupt INT0 occurs. LEDs should flash when interrupt INT1 occurs.

Interfacing Experiments

6. Interface LCD with the microcontroller. Display your name on the LCD.
7. Interface ADC0808 with 89C51 microcontroller. Write program to read analog voltage applied at the input of ADC. Display it on LCD.

PIC Micro controller

IO Programming

8. Introduction to Software Tools MPLAB, PROTEUS, and QL-2006 programmer.
9. Delay Loops Applications Flasher & Counter

Interrupts and Timer application

10. TMR0 Application Counter Using TMR0
11. Interrupt Application Controlling flashing speed of a flasher
12. EEPROM Memory Application

Interfacing Experiments

13. Application for Keypad and LCD
14. Analog Digital Conversion
15. Pulse-width modulation (PWM)

P: 45 Total: 45 Hrs

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P13EST201 REAL TIME OPERATING SYSTEMS

L	T	P	C
3	0	0	3

UNIT I REVIEW OF OPERATING SYSTEMS 9

Basic Principles – System Calls – Files – Processes – Design and Implementation of processes – Communication between processes – Operating System structures.

UNIT II DISTRIBUTED OPERATING SYSTEMS 9

Topology – Network types – Communication – RPC – Client server model – Distributed file system – Design strategies.

UNIT III REAL TIME MODELS AND LANGUAGES 9

Event Based – Process Based and Graph based Models – Petrinet Models – Real Time Languages – RTOS Tasks – RT scheduling - Interrupt processing – Synchronization – Control Blocks – Memory Requirements.

UNIT IV REAL TIME KERNEL 9

Principles – Design issues – Polled Loop Systems – RTOS Porting to a Target – Comparison and study of various RTOS like QNX – VX works – PSOS – C Executive – Case studies.

UNIT V RTOS APPLICATION DOMAINS 9

RTOS for Image Processing – Embedded RTOS for voice over IP – RTOS for fault Tolerant Applications – RTOS for Control Systems.

L: 45 Total: 45 Hrs

REFERENCES:

1. Herma K., "Real Time Systems – Design for distributed Embedded Applications", Kluwer Academic, 2000.
2. Charles Crowley, "Operating Systems-A Design Oriented approach" McGraw Hill 2005.
3. C.M. Krishna, Kang, G.Shin, "Real Time Systems", McGraw Hill, 2000.
4. Raymond J.A.Bhur, Donald L.Bailey, "An Introduction to Real Time Systems", PHI 2006.
5. Intel Manual on 16 bit embedded controllers, Santa Clara, 2005.

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P13EST202 EMBEDDED CONTROL SYSTEMS

L	T	P	C
3	0	0	3

UNIT I CONTROL OF HARDWARE AND SOFTWARE 6

Controlling the hardware with software – Data lines – Address lines - Ports – Schematic representation – Bit masking – Programmable peripheral interface –Switch input detection – 74 LS 244

UNIT II INPUT-OUTPUT DEVICES 8

Keyboard basics – Keyboard scanning algorithm – Multiplexed LED displays – Character LCD modules – LCD module display – Configuration – Time-of-day clock– Timer manager - Interrupts - Interrupt service routines – IRQ - ISR – Interrupt vector or dispatch table multiple-point - Interrupt-driven pulse width modulation.

UNIT III D/A AND A/D CONVERSION 12

R 2R ladder - Resistor network analysis - Port offsets - Triangle waves analog vs. digital values - ADC0809 – Auto port detect - Recording and playing back voice - Capturing analog information in the timer interrupt service routine - Automatic, multiple channel analog to digital data acquisition.

UNIT IV ASYNCHRONOUS SERIAL COMMUNICATION 9

Asynchronous serial communication – RS-232 – RS-485 – Sending and receiving data – Serial ports on PC – Low-level PC serial I/O module - Buffered serial I/O.

UNIT V CASE STUDIES: EMBEDDED C PROGRAMMING 10

Multiple closure problems – Basic outputs with PPI – Controlling motors – Bidirectional control of motors – H bridge – Telephonic systems – Stepper control –Inventory control systems.

L: 45 Total: 45 Hrs

REFERENCES:

1 Jean J. Labrosse, "Embedded Systems Building Blocks: Complete and Ready- To-Use Modules in C"The publisher, Paul Temme, 1999.

2 Ball S.R., 'Embedded microprocessor Systems – Real World Design', Prentice Hall, 1996.

3 Herma K, "Real Time Systems – Design for distributed Embedded Applications", Kluwer Academic, 1997.

4 Daniel W. Lewis, "Fundamentals of Embedded Software where C and Assembly meet", PHI, 2002.

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P13EST203 ADVANCED OPTIMIZATION TECHNIQUES

L	T	P	C
3	0	0	3

UNIT I INTRODUCTION 9

Introduction to Optimization- Concept of System and State- Performance Measure- Design Constraints- Condition for Optimality- Formulation of Objective Function-Classification of Optimization Problems.

UNIT II NONLINEAR OPTIMIZATION TECHNIQUES 9

Optimization Techniques- Single Variable and Multi-Variable Optimization Techniques and Unconstrained Minimization- Golden section- Random Pattern and Gradient Search Methods- Interpolation Methods- Optimization with Equality and Inequality Constraints- Direct Methods- Indirect Methods using Penalty Functions- Lagrange Multiplier- Geometric Programming and Stochastic Programming.

UNIT III GENETIC ALGORITHM 9

Introduction to Evolutionary Computing- Genetic Algorithm- Biological Inspiration –Finer Evaluation- Selection methods- Reproduction- Genetic Operators- Cross Over- Mutation- Schema Processing- Fitness Scaling- Advanced Genetic Operators and Techniques in Genetic Search- Constrained Genetic Algorithms- Penalty Functions- Multi Objective Optimization- Applications in Pattern Recognition Computers, Communication and Signal Processing.

UNIT IV SIMULATED ANNEALING 9

Simulated Annealing- Algorithm- Initial Solution- Assess Solution- Randomly Tweak Solution- Acceptance Criteria- Temperature Schedule- Adjusting Algorithm Parameters-Application

UNIT V - ANT COLONY OPTIMIZATION AND TABU SEARCH 9

Ant Colony Optimization – Ant Algorithm- Natural Motivation- Initial Population- Ant Movement- Ant Town- Pheromone Evaporation – Adjusting Algorithm Parameters- Alpha(α)/Beta(β)/ Rho(ρ)- Number of Ants- Applications- Routing- Shortest Term Problem. Tabu Search- Principles- Short Term Memory- Long Term Memory- Tabu Thresholding- Special Dynamic Tabu Tenure Strategies- Hash Function.

L: 45 Total: 45 Hrs

REFERENCES

1. Kalyonmoy Deb, “Optimization for Engineering Design”, Prentice Hall of India Ltd., 1991.
2. Pierre. D.A., “Optimization Theory with Applications”, John Wiley, 1969.
3. Rao.S.S., “Optimization Theory and Applications”, Wiley Eastern Ltd., 1979.
4. David.E.Goldberg, “Genetic Algorithms in Search, Optimization and Machine Learning”, International Student Edition, Addison Wesley Ltd., 1999.
5. Fred Glover, Manuel Laguna, “Tabu Search”, Kluwer Academic Publishers,1997.
6. Tim Jones.M, “Artificial Intelligence Application Programming”, Dreamtech Press, New Delhi, 2003.

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P13EST204	VLSI ARCHITECTURE AND DESIGN METHODOLOGIES	L	T	P	C
		3	0	0	3

UNIT I VLSI DESIGN METHODOLOGIES 9

Overview of digital VLSI design methodologies – Trends in IC Technology – Advanced Boolean algebra – Shannon's expansion theorem – Consensus theorem – Octal designation- Run measure – Buffer gates - Gate expander – Reed Muller expansion – Synthesis of multiple output combinational logic circuits by product map method – Design of static hazard free, dynamic hazard free logic circuits.

UNIT II ANALOG VLSI AND HIGH SPEED VLSI 9

Introduction to analog VLSI – realization of neural networks and switched capacitor filters – Sub-micron technology and Gas VLSI Technology.

UNIT III PROGRAMMABLE ASICS 9

Anti fuse – static RAM – EPROM and technology – PREP bench marks – Actel ACT – Xilinx LCA – Altera flex – Altera MAX DC & AC inputs and outputs – Clock and power inputs – Xilinx I/O blocks.

UNIT IV PROGRAMMABLE ASIC DESIGN SOFTWARE 9

Actel ACT – Xilinux LCA – Xilinux CPLD – Altera MAX 5000 and 7000 – Altera MAX 9000 – design systems – logic synthesis – half gate – schematic entry – Low level design language – PLA tools – EDIF – CFI design representation.

UNIT V LOGIC SYNTHESIS, SIMULATION AND TESTING 9

Basic features of VHDL language for behavioral modeling and simulation – Summary of VHDL data types – Dataflow and structural modeling – VHDL and logic synthesis – Circuit and layout verification – Types of simulation – Boundary scan test – Fault simulation – Automatic test pattern generation – design examples.

L: 45 Total: 45 Hrs

REFERENCES

1. William I.Fletcher, "An Engineering Approach to Digital Design", Prentice Hall of India.
2. Amar Mukharjee, "Introduction to NMOS and CMOS VLSI System Design", Prentice Hall, 1986.
3. M.J.S. Smith, "Application – specific integrates circuits", Addison Wesley Longman Inc. 1997.
4. Frederick J.Hill and Gerald R.Peterson, "Computer Aided Logical Design with emphasis on VLSI".

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P13ESP201	EMBEDDED SYSTEM LABORATORY II	L	T	P	C
		0	0	3	1

LIST OF EXPERIMENTS:

1. Write a program to demonstrate I/O operation of ARM kit using LED.
2. Write a program to interface seven segment displays to ARM kit.
3. Write a program to interface LCD to ARM kit.
4. Write an ALP to find the GCD (Greatest Common Divisor), with and without conditional execution of ARM instructions.
5. Write a program to multiply two matrices with and without MLA instruction.
6. Write a program to scan the keypad, assign own values to the keys and display the key pressed.
7. Write a program for convolution of two sequences with and without MLA instruction.
8. I/O programming, ADC/DAC, Timers, Interrupts
9. Design with Programmable Logic Devices using Xilinx/Altera FPGA and CPLD. Design and Implementation of simple Combinational/Sequential Circuits

P: 45 Total: 45 Hrs

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P13ESP301 EMBEDDED SYSTEM LABORATORY III

L	T	P	C
0	0	3	1

LIST OF EXPERIMENTS:

Write DSP program for TMS320C6713 using CCS

1. Correlation,
2. Convolution,
3. Arithmetic adder,
4. Multiplier,
5. Design of Filters – FIR based , IIR based
6. Hardware project **(On their own interest)**

P: 45 Total: 45 Hrs

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P13ESTE01 / P13PETE01 INTELLIGENT CONTROL

L	T	P	C
3	0	0	3

UNIT I SYSTEMS AND APPROACHE 9

Approaches to intelligent control. Architecture for intelligent control. Symbolic reasoning system, rule-based systems, the AI approach. Knowledge representation. Expert systems.

UNIT II ARTIFICIAL NEURAL NETWORKS 9

Concept of Artificial Neural Networks and its basic mathematical model, McCulloch- Pitts neuron model, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron. Learning and Training the neural network. Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations. Hopfield network, Self-organizing network and Recurrent network. Neural Network based controller

UNIT III GENETIC ALGORITHM 9

Basic concept of Genetic algorithm and detail algorithmic steps, adjustment of free parameters. Solution of typical control problems using genetic algorithm. Concept on some other search techniques like tabu search and ant-colony search techniques for solving optimization problems.

UNIT IV FUZZY LOGIC SYSTEM 9

Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning. Introduction to fuzzy logic modeling and control. Fuzzification, inferencing and defuzzification. Fuzzy knowledge and rule bases. Fuzzy modeling and control schemes for nonlinear systems. Self-organizing fuzzy logic control. Fuzzy logic control for nonlinear time-delay system.

UNIT V FL AND NN APPLICATIONS 9

GA application to power system optimisation problem, Case studies: Identification and control of linear and nonlinear dynamic systems using Matlab-Neural Network toolbox. Stability analysis of Neural-Network interconnection systems. Implementation of fuzzy logic controller using Matlab fuzzy-logic toolbox. Stability analysis of fuzzy control systems.

L: 45 Total: 45 Hrs

REFERENCES:

1. Jacek.M.Zurada, "Introduction to Artificial Neural Systems", Jaico Publishing House, 2005.
2. KOSKO, B. "Neural Networks And Fuzzy Systems", Prentice-Hall of India Pvt. Ltd., 2008.
3. KLIR G.J. & FOLGER T.A. "Fuzzy sets, uncertainty and Information", Prentice-Hall of India Pvt. Ltd., 2003.
4. Zimmerman H.J. "Fuzzy set theory-and its Applications"-Kluwer Academic Publishers, 2004.

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P13ESTE02 / P13PETE02 ADVANCED DIGITAL SIGNAL PROCESSING

L	T	P	C
3	0	0	3

UNIT I DISCRETE TIME SIGNALS AND SYSTEMS 9

Representation of discrete time signal – classifications – Discrete time – system – Basic operations on sequence – linear – Time invariant – causal – stable – solution to difference equation – convolution sum – correlation – Discrete time Fourier series – Discrete time Fourier transform.

UNIT II FOURIER AND STRUCTURE REALIZATION 9

Discrete Fourier transform – properties – Fast Fourier transform – Z-transform – structure realization – Direct form – lattice structure for FIR filter – Lattice structure for IIR Filter.

UNIT III FILTERS 9

FIR Filter – windowing technique – optimum equiripple linear phase FIR filter – IIR filter – Bilinear transformation technique – impulse invariance method – Butterworth filter – Tchebyshev filter.

UNIT IV MULTISTAGE REPRESENTATION 9

Sampling of band pass signal – antialiasing filter – Decimation by a n integer factor – interpolation by an integer factor – sampling rate conversion – implementation of digital filter banks – sub-band coding – Quadrature mirror filter – A/D conversion – Quantization – coding – D/A conversion – Introduction to wavelets.

UNIT V DIGITAL SIGNAL PROCESSORS 9

Fundamentals of fixed point DSP architecture – Fixed point number representation and computation – Fundamentals of floating point DSP architecture – floating point number representation and computation – study of TMS 320 C 50 processor – Basic programming – addition – subtraction – multiplication – convolution – correlation – study of TMS 320 C 54 processor – Basic programming – addition – subtraction – multiplication – convolution – correlation.

L: 45 Total: 45 Hrs

REFERENCES:

1. John G.Proakis, Dimitris G.Manolakis, "Digital Signal Processing: Principles, Algorithms and Applications", PHI 1997 Edition 3.
2. S.Salivahanan, A.Vallavaraj and C.Gnanapriya "Digital Signal Processing", TMH, 2000.
3. A.V. Oppenheim and R.W.Schafer, Englewood "Digital Signal Processing", Prentice- Hall, Inc, 1975.
4. Rabiner and Gold, "Theory and Application of Digital Signal Processing", A comprehensive, Industrial – Strength DSP reference book 1998 PHI
5. B.Venkatramani & M.Bhaskar, "Digital Signal Processors architecture, Programming and Applications", TMH, 2002.

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P13ESTE03 / P13PETE03 **VHDL**

L	T	P	C
3	0	0	3

UNIT I VHDL FUNDAMENTALS 9

Fundamental Concepts – Modeling Digital Systems – Domains and Levels of Modeling – Modeling Languages – VHDL Modeling concepts – Scalar Data Types and Operations – Constants and variables – Scalar Types – Type Classification – Attributes and Scalar types – Expressions and operators – Sequential Statements – If statements – Case statements – Null Statements – Loop statements – Assertion and Report statements.

UNIT II COMPOSITE DATA TYPES AND BASIC MODELING CONSTRUCTS 9

Arrays – Unconstrained Array types – Array Operations and Referencing – Records – Basic Modeling Constructs – Entity Declarations – Architecture Bodies – Behavioral Descriptions – Structural Descriptions – Design Processing. Case Study: A pipelined Multiplier Accumulator.

UNIT III SUBPROGRAMS AND PACKAGES 9

Procedures – Procedure Parameters – Concurrent Procedure Call Statements – functions – Overloading – Visibility of Declarations – Packages and Use Clauses – Package declarations – Package bodies – Use Clauses – The predefined – Aliases - Aliases for data objects – Aliases for Non-Data Items. Case Study: A Bit-Vector Arithmetic Package.

UNIT IV SIGNALS, COMPONENTS, CONFIGURATIONS 9

Basic Resolved signals – IEEE Std_Logic_1164 Resolved subtypes – Resolved signal parameters – Generic Constants – Parameterizing behavior – Parameterizing structure – Components and Configurations – Components – Configuring component Instances – Configuration Specification – Generate Statements – generating iterative structure – Conditionally generating structures – Configuration of generate Statements. Case Study: The DLX Computer System.

UNIT V ADTs AND FILES 9

Access Types – Linked Data structures – Abstract Data Types using Packages – Files and Input/Output – Files – The Package Textio – Verilog. Case Study: Queuing Networks.

L: 45 Total: 45 Hrs

REFERENCES:

1. Peter J. Ashenden, The Designer's Guide to VHDL, Morgan Kaufmann Publishers, San Francisco, Second Edition, May 2001.
2. Zainalabedin Navabi, VHDL Analysis and Modeling of Digital Systems, McGraw Hill International Editions, Second Edition, 1998.
3. James M.Lee, Verilog Quick start, Kluwer Academic Publishers, Second Edition, 1999.

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P13ESTE04 / P13PETE04 VLSI DESIGN

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UNIT I VLSI DESIGN METHODOLOGY & MOS TECHNOLOGY 9

VLSI Design process — Architectural Design — Logical design — Physical design — Layout styles — Full custom — Semicustom approaches - An overview of wafer fabrication — Wafer processing — Oxidation — Patterning — Diffusion — Ion implantation — Deposition — Silicon gate nMOS process — CMOS processes — nWeIl — pWell — Twintub — Silicon on insulator.

UNIT II ELECTRICAL PROPERTIES OF MOS AND CMOS CIRUITS 9

MOS enhancement transistor — PMOS enhancement transistor — Threshold voltage — Threshold voltage equations — MOS device equations — Basic DC equations — Second order effects — MOS modules — Small signal AC characteristics — Nmos inverter— Steered Input to an nMOS inverter — Depletion mode and enhancement mode pullups — CMOS inverter — DC characteristics — Inverter delay — Pass transistor — Transmission gate.

UNIT III MOS AND CMOS CIRCUIT DESIGN PROCESSES 9

CMOS process enhancements — Interconnect - Circuit elements - Latchup – Latchup prevention techniques - Need for Layout design rules — Mead conway design rules for the silicon gate nMOS process — CMOS nWelllpWell design rules — Simple Layout examples — Sheet resistance — Area capacitance — Wiring Capacitance — Drive large capacitive loads.

UNIT IV LOGIC DESIGN 9

Switch Logic — Pass Transistor and transmission gate — Gate Logic — Iriverter — Two input NAND gate — NOR gate — Other forms of CMOS logic — Dynamic CMOS logic — Clocked CMOS logic — Precharged domino CMOS logic — Structured design — Simple combinational logic design examples — Parity generator — Multipiexers — locked sequential circuits —Two phase clocking — Charge storage — Dynamic register element — nMOS and CMOS — Dyrimic shift register — Semi static register — JK flip flop circuit.

UNIT V TESTING 9

Importance of testing – Boundary – Scan Test – fauits – fault simulation – Automatic Test – Pattern Generation – IDDQ Test – Built – in Self Test – A simple test example..

L: 45 Total: 45 Hrs

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REFERENCES:

1. Douglas A Pucknell and Kamran Eshrarigian, 'Basic VLSI Design; Prentice Hall of India, New Delhi, Ill Edition, 1999.
2. Neil H B West and Kamran Eshranghian, 'Principles of CMOS VLSI Design: A system perspective Addison-Wesley, II Edition, II Indian Reprint, 2000.
3. Amar Mukherjee, 'Introduction to nMOS and CMOS VLSI system design: Prentice Hail, USA, 1996.
4. Wayne Wolf, 'Modem VLSI Design: Systems on Si1icon II Edition, Pearson Education, III Indian Reprint, 2001.
5. Eugene D Fabricous, 'Introduction to VLSI design: McGrawHill International Edition,1990.

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P13ESTE05 ADVANCED EMBEDDED SYSTEMS

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UNIT I PRINCIPLES OF EMBEDDED SYSTEM 9

Introduction - Embedded systems description, definition, design considerations & requirements - Overview of Embedded system Architecture - Categories of Embedded Systems - Product specifications - hardware/software partitioning - iterations and implementation - hardware software integration - product testing techniques. Wired Communication Protocols: UART - Inter Integrated Circuit (I2C)- Serial Peripheral Interface (SPI) - Controller Area Network (CAN).Wireless communication Protocols: Zigbee Protocols – Blue tooth Protocols - IrDA.

UNIT II ARM PROCESSOR FUNDAMENTALS 9

ARM core Introduction – Registers – Current Program Status Register – Pipeline –Exception – Interrupts – Vector Table – Core Extension – Architecture Revisions –ARM Processor Families – ARM Instruction Set – Thumb Instruction set – Thumb Register Usuage – ARM – Thumb Interworking – Stack Instruction – Software Interrupt Instruction.

UNIT III CACHES AND MMU 9

The Memory Hierarchy and Cache Memory – Cache Architecture - Cache Policy –Co Processor and Caches – Flushing and Cleaning Cache Memory – Cache Lockdown – Caches and Software Performance. MMU: Moving from an MPU to an MMU – Virtual Memory – Details of ARM MMU – The Caches and Write Buffer – Co Processor and MMU configuration.

UNIT IV OPTIMIZED PRIMITIVES 9

Double Precision Integer Multiplication – Integer Normalization and count Leading Zeros – Division – Square Roots – Transcendental Functions: Log,,exp,sin,cos – Endian Reversal and Bit Operations – Saturated and Rounded Arithmetic – Random Number Generation.

UNIT V WRITING AND OPTIMIZING ARM ASSEMBLY CODE 9

Writing Assembly Code – Profiling and Cycle Counting – Instruction Scheduling –Register Allocation – Conditional Execution – Looping Constructs – Bit Manipulation – Efficient Switches – Handling Unaligned Data.

L: 45 Total: 45 Hrs

REFERENCES

1. Andrew N.Sloss, Dominic Symes, Chris Wright, “ARM System Developer’s Guide”, Morgan Kaufmann Series in Computer Architecture and Design, 2004.
2. Tammy Noergaard, “Embedded Systems Architecture”, Newnes, 2005.
3. David Seal, “ARM Architecture Reference Manual”, 2005.
4. Steve Furbe, “ARM System-on-Chip Architecture”, Addison-Wesley Professional, 2nd Edition, 2000.

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P13ESTE06	SOFTWARE TECHNOLOGY FOR EMBEDDED SYSTEMS	L	T	P	C
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UNIT I PROGRAMMING EMBEDDED SYSTEMS 9

Embedded Program – Role of Infinite loop – Compiling, Linking and locating – downloading and debugging – Emulators and simulators processor – External peripherals – Toper of memory – Memory testing – Flash Memory.

UNIT II OPERATING SYSTEM 9

Embedded operating system – Real time characteristics – Selection process – Flashing the LED – serial ports – Zilog 85230 serial controlled code efficiency – Code size – Reducing memory usage – Impact of C++.

UNIT III HARDWARE FUNDAMENTALS 9

Buses – DMA – interrupts – Built-ins on the microprocessor – Conventions used on schematics – Microprocessor Architectures – Software Architectures – RTOS Architectures – Selecting Architecture.

UNIT IV RTOS 9

Tasks and Task states – Semaphores – Shared data – Message queues, Mail boxes and pipes – Memory management – Interrupt routines – Encapsulating semaphore and queues – Hard Real-time scheduling – Power saving.

UNIT V EMBEDDED SOFTWARE DEVELOPMENT TOOLS 9

Host and target machines – Linkers / Locators for Embedded Software – Debugging techniques – Instruction set simulators Laboratory tools – Practical example – Source code.

L: 45 Total: 45 Hrs

REFERENCES

1. David E.Simon: An Embedded Software Primer Perason Education, 2003.
2. Michael Bass: Programming Embedded Systems in C and C++ Oreilly, 2003.
3. Raymond J.A.Bhur, Donald L.Bailey, “An Introduction to Real Time Systems”, PHI 2006.
4. Rajkamal, “embedded system architecture, programming and design”Tata McGraw hill, 2003.
5. Frank vahid, Tony Givargas, “Embedded system Design- a unified hardware/ software introduction” John Willy, 2002.

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P13ESTE07 EMBEDDED SENSOR NETWORKS

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UNIT 1 SENSOR NETWORKS 9

Over view of sensor networks - Constraints and Challenges – Advantages of sensor networks – Applications – Collaborative Processing – Key definitions in sensor networks – Tracking scenario – Problem formulation –Distributed representation and interference of states – Tracking multiple objects – Sensor models – performance comparison and metrics.

UNIT 2 NETWORKING SENSORS 9

Key assumptions – Medium access control – S-MAC Protocol – IEEE 802.15.4 standard and ZigBee – General Issues – Geographic, Energy-Aware Routing – Attribute based routing

UNIT 3 INFRASTRUCTURE ESTABLISHMENT 9

Topology control – Clustering-Time synchronization – Localization – Task driven sensing- Role of sensor nodes – Information based tasking – Routing and aggregation

UNIT 4 SENSOR NETWORK DATABASE 9

Sensor Database Challenges – Querying the physical environment – Interfaces – In-network aggregation – Data centric storage – Data indices and range queries – Distributed Hierarchical aggregation – Temporal data.

UNIT 5 SENSOR NETWORK PLATFORMS AND TOOLS 9

Sensor Node Hardware – Sensor network programming challenges – Node level software platforms- Operating system TinyOS – Node level simulators – State centric programming- Applications and future directions.

L: 45 Total: 45 Hrs

REFERENCES

1. Feng Zhao, Leonidas Guibas, "Wireless Sensor Networks An information processing approach", Mogan Kanufmann Publishers, 2004
2. Richard Zurawski, "Embedded System Hand Book", CRC Press, 2006
3. Iran Stojmenovic, "Hand book of sensor networks", John Wiley & Sons Inc., 2005.
4. Michel Banatre, Pedre Jose Marron, Anibal Ollero and Adam Wilisz, "Cooperating Embedded System and Wireless sensor Network' John Willy, 2008.

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P13ESTE08 EMBEDDED PROCESSORS

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UNIT I ARM EMBEDDED SYSTEMS 9

ARM Embedded Systems – Design Philosophy –Systems Hardware – Systems Software – ARM processor fundamentals – ARM processor families.

UNIT II ARM PROGRAMMING 9

ARM Instruction Set – The Thumb Instruction Set- Exception and Interrupt handling – Firmware - Example programs with embedded operating system for ARM.

UNIT III ARM DSP 9

ARM Digital Signal Processing – Introduction to DSP on the ARM – FIR – IIR – DFT Exception and Interrupt Handling ARM Memory Managements Unit.

UNIT IV BALACFIN PROCESSOR 9

Introduction to BALACFIN processor : Embedded Processor – Micro signal Architecture – Real time embedded signal processing - Architecture – Software tools –Number formats - Overview of signal acquisition and transfer to memory- DMA operations - Using cache – Scratchpad memory of BALACFIN processor- power management.

UNIT V PRACTICAL DSP APPLICATIONS 9

Overview of Real time processing - Signal generator with Balackfin processor -Implementation of FIR – IIR filters – Graphic equalizer - Audio coding and audio effects – Digital Image processing.

L: 45 Total: 45 Hrs

REFERENCES

1. Bary B. Brey, "The Intel Microprocessors Architecture , Programming and Interfacing", Prentice Hall of India Pvt Ltd – New Delhi – 2006
2. Andrew Sloss, Dominic Symes, and Chris Wright," ARM System Developer's Guide: Designing and Optimizing System" , The Morgan Kaufmann Series, 2004
3. Woon-Seng Gan ,Sen M. Kuo, "Embedded Signal Processing with the Micro Signal Architecture" John Wiley & sons Inc, Hoboken, New jersey, 2007
4. Jason Andrews,"Co-verification of Hardware and Software for ARM SoC Design (Embedded Technology)" , Newnes – 2004

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P13ESTE09 **EMBEDDED NETWORKING**

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UNIT I EMBEDDED NETWORKING 9

Embedded networking – code requirements – Communication requirements – Introduction to CAN open – CAN open standard – Object directory – Electronic Data Sheets & Device – Configuration files – Service Data Objectives – Network management CAN open messages – Device profile encoder.

UNIT II CONTROLLER AREA NETWORKS 9

CAN open configuration – Evaluating system requirements choosing devices and tools – Configuring single devices – Overall network configuration – Network simulation – Network Commissioning – Advanced features and testing.

UNIT III CAN CONTROLLER AND DEVELIOPMENT TOOLS 9

Controller Area Network – Underlying Technology CAN Overview – Selecting a CAN Controller – CAN development tools.

UNIT IV IMPLEMENTATION OF CAN 9

Implementing CAN open Communication layout and requirements – Comparison of implementation methods – Micro CAN open – CAN open source code –Conformance test – Entire design life cycle.

UNIT V IMPLEMENTATION ISSUES 9

.Implementation issues – Physical layer – Data types – Object dictionary – Communication object identifiers – Emerging objects – Node states.

L: 45 Total: 45 Hrs

REFERENCES

1 Glaf P.Feiffer, Andrew Ayre and Christian Keyold "Embedded Networking with CAN and CAN open" Embedded System Academy 2005.

2 Peter Barry and Gerard Hartnett, "Designing Embedded Networking Application", Intel Press, 2006

3 Gregory Pottie and William Kaiser, "Principle of Embedded Network System Design", Cambridge University Press, 2005.

4 Jason Andrews,"Co-verification of Hardware and Software for ARM SoC Design (Embedded Technology)" , Newnes – 2004

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P13ESTE10 MICRO ELECTRO MECHANICAL SYSTEMS

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UNIT I MEMS DEVICES 9

Piezoresistive pressure sensor- Piezoresistive Accelerometer - Capacitive Pressure Sensor- Accelerometer and Microphone - Resonant Sensor and Vibratory Gyroscope - Micro Mechanical Electric and Optical Switches-Micro Mechanical Motors - Micro Electro Mechanical Systems Analysis and Design of MEMS Devices- MEMS applied to rehabilitation engineering- Nano Sensors.

UNIT II BASIC MECHANICS OF BEAM AND DIAPHRAGM STRUCTURES 9

Stress and Strain- Stress and Strain of Beam Structures-Vibration Frequency by Energy Methods Vibration Modes and the Buckling of a Beam- Damped and forced vibration-Basic Mechanics of Diaphragms – Problems.

UNIT III AIR DAMPING AND ELECTRO STATIC ACTUATION 9

Drag Effect of a Fluid- Squeeze-film Air Damping-Damping of Perforated Thick Plates-Slide-film Air Damping- Damping in Rarefied –Air Problems- Electro static Forces-Electrostatic Driving of Mechanical Actuator Step and Alternative-Driving –Problems.

UNIT IV CAPACITIVE SENSING AND EFFECTS OF ELECTRICAL EXCITATION 9

Capacitive Sensing Schemes- Effects of Electrical Excitation: Static Signal- Effects of Electrical Excitation: Step Signal –Effects of Electrical Excitation: Pulse Signal –Problems.

UNIT V PIEZO RESISTIVE SENSING 9

Piezoresistive Effect of Silicon-Coordinate Transformation of Second Rank Tensors-Coordinate Transformation of Piezoresistive Coefficient –Piezoresistive Sensing Elements-Polysilicon Piezoresistive Sensing Elements-Analyzing-Piezo resistive Bridge-Problems.

L: 45 Total: 45 Hrs

REFERENCES

1. Minhang Bao , **“** Analysis and design principles of MEMS devices”, Elsevier Publications, 2005,USA.
2. Nadim Maluf and Kirt Williams, “An Introduction to Micro Electro Mechanical Systems Engineering, Second Edition”, Artech House Publishers, June 2004, USA.
3. Gabriel M. Rebeiz , “RF MEMS: Theory, Design, and Technology”, Wiley-Interscience; 1st edition, 2002,UK.
4. John A. Pelesko and David H. Bernstein, “ Modeling MEMS and NEMS”, CRC Press, 2002,UK

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P13ESTE11 **ASIC DESIGN**

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UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN 9

Types of ASICs – Design Flow – CMOS transistors, CMOS design rules – Combinational Logic Cell – Sequential logic cell – Data path logic cell – Transistors as Resistors –Transistor Parasitic Capacitance – Logical effort – Library cell design – Library architecture.

UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMBALE ASIC I/O CELLS 9

Anti fuse – static RAM – EPROM and EEPROM technology – PREP bench marks –Actel ACT – Xilinx LCA – Altera FLEX – Altera MAX DC & AC inputs and outputs –Clock and power inputs – Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY 9

Actel ACT – Xilinx LCA – Xilinx EPLD – Altera MAX 5000 and 7000 – Altera MAX 9000 Altera FLEX – Design systems – Logic Synthesis – Half Gate ASIC – Schematic entry – Low level design language – PLA tools – EDIF – CFI design representation.

UNIT IV LOGIC SYNTHESIS, SIMULATION AND TESTING 9

Verilog and logic synthesis – VHDL and logic synthesis - Types of simulation – Boundary scan test – Fault simulation – Automatic test pattern generation.

UNIT V ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING 9

System partition – FPGA partitioning – partitioning methods – floor planning – placement – physical design flow – global routing – detailed routing – special routing – circuit extraction – DRC.

L: 45 Total: 45 Hrs

REFERENCES

1. M.J.S. SMITH, “Application – Specific Integrated Circuits” – Addison – Wesley Longman Inc., 1997.
2. Andrew Brown, “VLSI Circuits and Systems in Silicon”, McGraw Hill, 1991.
3. S.D.Brown, R.J.Francis, J.Rox, Z.G.Uranesic, “Field Programmable Gate Arrays”–Kluever Academic Publishers, 1992.
4. Mohammed Ismail and Terri Fiez, “Analog VLSI Signal and Information Processing”, McGraw Hill, 1994.
5. S.Y. Kung, H.J.Whilo House, T.Kailath, “VLSI and Modern Signal Processing”, Prentice Hall, 1985.
6. Jose E.France, Yannis Tsividis, “Design of Analog – Digital VLSI Circuits for Telecommunication and Signal Processing”, Prentice Hall, 1994

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P13ESTE12 SYSTEM SIMULATION AND MODELING

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UNIT I SYSTEM AND SYSTEM ENVIRONMENT 9

Concept of a system-continuous and discrete systems – models of a system –modeling approaches – advantages and disadvantages of simulation systems-steps in simulation study-point estimates, confidence interval.

UNIT II PROBABILITY CONCEPTS IN SIMULATION 9

Random number generation-mid square-mid product method-constant multiplier method-additive congruental method-linear congruential method test for random numbers-the Chi square test – the Kolmogrov- Smimov test – Runs test-Gaps test-Random variable generation – Distribution – exponential, Poisson , Uniform, Weibull-Empirical distribution-Normal distribution – building on empirical distribution – rejection method.

UNIT III STATE SPACE BASED MODELS 9

Markovian-Non Markovian models – Discrete and Continuous time Markov Chains – Markov reward models – Semi Markov models – Markov regenerative models.

UNIT IV NON STATE SPACE METHODS 9

Performance models – queueing models – task precedence graphs – Dependability models – Reliability graphs – Fault tress.

UNIT V PETRI NET MODEL 9

Finite state Automata – Petri nets – Stochastic Petri nets – Stochastic Reward nets – Colored Petri nets – Fluid Petri nets.

L = 45 Total=45 Hrs

REFERENCES

1. Geoffrey Gordon,"Systems Simulation", Prentice Hall of India, II Edition, 1992.
2. Kishore.S.Trivedi, "Probability and Statistics with Reliability, Queuing and Computer Science Applications", John Wiley and Sons, 2001.
3. Gotrifed B.S.,"Elements of Stochastic Process Simulation", Prentice Hall, 1984.
4. Arson J.S.,Banks J.C., and Nelson B.L., "Discrete Event Systems Simulation", Prentice Hall of India, 1996.
5. Ajmone Marsan M., Kartson DF., Conte G. and Donatelli S., "Modeling with Generalized Stochastic Petri Nets", Willey, New York, 1995.
6. Kleinrock L., "Queueing Systems Theory",Vol.I, Kluwer Academic Press, 1995

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P13ESTE13 **DIGITAL IMAGE PROCESSING**

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UNIT I DIGITAL IMAGE FUNDAMENTALS 9

Image Representation - gray scale and colour Images, image sampling and quantization. Two dimensional orthogonal transforms - DFT, WHT, Haar transform, KLT, DCT- Introduction to transforms on Image and video processing.

UNIT II IMAGE ENHANCEMENT AND EDGE DETECTION 9

Image Enhancement - filters in spatial and frequency domains, histogram-based processing, homomorphic filtering. Edge Detection - non parametric and model based approaches, LOG filters, localisation problem- Segmentation -Introduction to Region Growing.

UNIT III IMAGE RESTORATION 9

Image Restoration - PSF, circulant and block - circulant matrices, deconvolution, restoration using inverse filtering, Wiener filtering and maximum entropy-based methods.

UNIT IV - MORPHOLOGICAL IMAGE PROCESSING 9

Mathematical Morphology - binary morphology, dilation, erosion, opening and closing, duality relations, gray scale morphology, applications such as hit-and-miss transform, thinning and shape decomposition.

UNIT V - IMAGE PROCESSING 9

Computer Tomography - parallel beam projection, Radon transform, and its inverse, Back-projection operator, Fourier-slice theorem, CBP and FBP methods, ART, Fan beam projection and applications.

L = 45 Total = 45 Hrs

REFERENCES

1. Milian Sonka, Vaclav Hlavac, Roger Boyle, "Image Processing, Analysis and Machine Vision", PWS Publishing, II Edition, 1999.
2. R.M. Haralick, and L.G. Shapiro, “Computer and Robot Vision”, Vol-1, Addison Wesley, Reading, MA, 1992.
3. R. Jain, R. Kasturi and B.G. Schunck, “Machine Vision”, McGraw-Hill International Edition, 1995.
4. A. Rosenfold and A. C. Kak, “Digital Image Processing”, Vols. 1 and 2, Prentice Hall, 1986.
5. H. C. Andrew and B. R. Hunt, “Digital Image Restoration”, Prentice Hall, 1977

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P13ESTE14 INDUSTRIAL AUTOMATION AND CONTROL

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UNIT I INTRODUCTION TO INDUSTRIAL AUTOMATION 9

Fundamentals of Industrial Automation and Control Elements- Principles and Strategies - Smart Sensors, Transducers and Motion Actuators- PID Controller- Digital Controller. Program of Instructions

UNIT II PROGRAMMABLE LOGIC CONTROLLERS 9

Process Controller- Relay Logic – Programmable Logic Controller- Basic Structure –Ladder Logic- Programming- PLC Internal Operation and Signal Processing- I/O Processing- Remote Access- Communication System for Industrial Automation- Intelligent System for Monitoring, Supervision and Control.

UNIT III COMPUTER NUMERIC CONTROL 9

Introduction to CNC Systems- Types –Analogue, Digital, Absolute and Incremental- Open Loop and Closed Loop - CNC Drives and Feedback Devices- Adaptive Control – CNC Part Programming.

UNIT IV AUTOMATED SYSTEMS 9

Fixed Automation – Programmable Automation – Flexible Automation - Material Transport Systems – Process Monitoring – Conveyor Systems – Cranes and Hoists – Automated Storage and Retrieval Systems – Automated Data Capture – Digital Factories.

UNIT V INDUSTRIAL APPLICATIONS 9

Industrial Control Applications- Cement Plant – Thermal Plant- Water Treatment Plant- Steel Plant- Irrigation Canal Management- Paper Industry.

L: 45 Total: 45 Hrs

REFERENCES

1. Krishna Kant, “Computer-Based Industrial Control”, Prentice Hall of India Pvt. Ltd., New Delhi, 2004.
2. Gray Dunning, “Introduction to Programmable Logic Controllers”, Delmar Publishers, 1998.
3. Frank D. Petruzella, “Programmable Logic Controllers”, Mc Graw Hill, Second Edition.
4. Richard L.Shell, Ernest L.Hall, “Hand Book of Industrial Automation”, Published by Marcel Dekker Inc., Society of Manufacturing Engineers.
5. Mikell P. Groover, “Automation, Production Systems and Computer Integrated Manufacturing”, Second edition Pearson Education, 2001.

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P13ESTE15 ADVANCED COMPUTER ARCHITECTURE

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UNIT I FUNDAMENTALS OF COMPUTER DESIGN 9

Review of fundamentals of CPU, Memory and IO – Performance evaluation – Instruction set principles – Design issues – Example Architectures.

UNIT II INSTRUCTION LEVEL PARALLELISM 9

Pipelining and handling hazards – Dynamic Scheduling – Dynamic hardware prediction – Multiple issue – Hardware based speculation – Limitations of ILP – Case studies.

UNIT III INSTRUCTION LEVEL PARALLELISM WITH SOFTWARE APPROACHES 9

Compiler techniques for exposing ILP – Static branch prediction – VLIW & EPIC – Advanced compiler support – Hardware support for exposing parallelism – Hardware versus software speculation mechanisms – IA 64 and ltanium processor.

UNIT IV MEMORY AND I/O 9

Cache performance – Reducing cache miss penalty and miss rate – Reducing hit time – Main memory and performance – Memory technology. Types of storage devices – Buses – RAID – Reliability, availability and dependability – I/O performance measures – Designing an I/O system.

UNIT V MULTIPROCESSORS AND THREAD LEVEL PARALLELISM 9

Symmetric and distributed shared memory architectures – Performance issues – Synchronization – Models of memory consistency – Multithreading.

L: 45 Total: 45 Hrs

REFERENCES

1. John L.Hennessey and David A.Patterson, “Computer Architecture: A Quantitative Approach”, Third Edition, Morgan Kaufmann, 2006.
2. D.Sia, T.Fountain and P.Kacsuk, “Advanced computer Architectures: A Design Space Approach”, Addion Wesley, 2000.\
3. Hessham EL- Rewni, Mostafa Abd- El – Barr, “Advanced computer Architecture and parallel processing”, John Willy, 2005.
4. Mark D Hill, Norman P Jouppi, Gurindar S Sohi, “Reading and Computer Architecture”, Morgan Kaufmann, 2000.

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P13ESTE16 DIGITAL CONTROL SYSTEMS

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UNIT I MODELLING OF DIGITAL SYSTEM 9

Types of signal – digital control systems – block diagram – quantization and quantization error – review of Z transform and its applications – Pulse transfer function – block diagrams – signal flow graphs – ZOH and its characteristics.

UNIT II ANALYSIS OF DIGITAL CONTROL SYSTEMS 9

Mapping of s plane and z plane – steady error analysis – root locus – polar plot – Nyquist stability criterion – Bode diagram – gain and phase – margins – Jury's stability test.

UNIT III DESIGN OF DIGITAL CONTROL SYSTEM 9

Design of continuous controllers with equivalent digital controllers – realization of digital controllers by digital programming – digital PID controller – design through Bilinear transformation – design in Z plane using root locus diagram – phase lead, phase lag, networks, PID, PD PI controllers.

UNIT IV STATE SPACE ANALYSIS OF DIGITAL CONTROL SYSTEMS 9

Concept of state space – state space representations of discrete systems – canonical forms – state transition matrix – properties – solution to homogeneous and non- homogeneous state equations.

UNIT V POLE PLACEMENT AND OBSERVER DESIGN 9

Controllability and observability of linear time invariant discrete systems – transforming state – space equations into canonical forms – design using pole placement – state observer – design of full order and reduced order state observers.

L: 45 Total: 45 Hrs

REFERENCES

1. M.Gopal, "Digital control Engineering", "New age International" 2009.
2. Katsuhiko Ogata,"Discrete-Time Control Systems", II Edition Pearson Education Asia, Singapore, 2001.
3. Benjamin C. Kuo,"Digital Control Systems", II Edition, Oxford University Press, 2004.
4. Gene F.Franklin J.David Powell and Michael Workman, "Digital Control of Dynamic Systems", III Edition, Addision Wesley Longman, 2005.
5. Charles L. Phillips and H.Troy Nagle , "Digital control system and analysis" 3rd Edition, Prentice Hall,2007

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P13ESTE17 **OPERATING SYSTEMS**

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UNIT – I- INTRODUCTION 9

Operating System Structure – Operating System Operations – Process Management – Memory Management – Storage Management – Protection and Security – Distributed Systems – Computing Environments – System Structures: Operating System Services – User Operating System Interface – System Calls – Types of System Calls – System Programs – Process Concept: Process Scheduling – Operations on Processes – Inter-process Communication.

UNIT – II- MULTITHREADED PROGRAMMING: 9

Overview – Multithreading Models – Threading Issues – Process Scheduling: Basic Concepts – Scheduling Criteria – Scheduling Algorithms – Multiple-Processor Scheduling – Synchronization – The Critical-Section Problem – Peterson's Solution – Synchronization Hardware – Semaphores – Classic problems of Synchronization – Monitors.

UNIT – III DEADLOCKS 9

System Model – Deadlock Characterization – Methods for Handling Deadlocks – Deadlock Prevention – Deadlock Avoidance – Deadlock Detection – Recovery from Deadlock – Memory Management Strategies: Swapping – Contiguous Memory Allocation – Paging – Structure of the Page Table – Segmentation.

UNIT - IV VIRTUAL MEMORY MANAGEMENT: 9

Demand Paging – Copy on Write – Page Replacement – Allocation of Frames – Thrashing – File System: File Concept – Access Methods – Directory Structure – File Sharing – Protection.

UNIT - V IMPLEMENTING FILE SYSTEMS: 9

File System Structure – File System Implementation – Directory Implementation – Allocation Methods – Free-space Management - Secondary Storage Structure: Disk Structure – Disk Scheduling – Disk Management – Swap-Space Management. Case Study: The Linux System.

L: 45 Total: 45 Hrs

REFERENCES

1. Abraham Silberschatz, Peter Baer Galvin and Greg Gagne, "Operating System Principles", John Wiley & Sons (ASIA) Pvt. Ltd, Seventh Edition, 2006
2. Harvey M. Deitel, "Operating Systems", Pearson Education Pvt. Ltd, Second Edition, 2002.
3. Andrew S. Tanenbaum, "Modern Operating Systems", Prentice Hall of India Pvt. Ltd, 2003.
4. William Stallings, "Operating System", Prentice Hall of India, Fourth edition, 2003.

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P13ESTE18	EMBEDDED COMMUNICATION SOFTWARE DESIGN	L	T	P	C
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UNIT 1 OSI REFERENCE MODEL 9

OSI Reference Model – Communication Devices – Communication Echo System – Design Consideration – Host Based Communication – Embedded Communication System – OS Vs RTOS.

UNIT 2 SOFTWARE PARTITIONING 9

Software Partitioning – Limitation of strict Layering – Tasks & Modules – Modules and Task Decomposition – Layer2 Switch – Layer3 Switch / Routers – Protocol Implementation – Management Types – Debugging Protocols.

UNIT 3 DATA STRUCTURES 9

Tables & other Data Structures – Partitioning of Structures and Tables – Implementation – Speeding Up access – Table Resizing – Table access routines – Buffer and Timer Management – Third Party Protocol Libraries.

UNIT 4 MANAGEMENT SCHEMES 9

Management Software – Device Management – Management Schemes – Router Management – Management of Sub System Architecture – Device to manage configuration – System Start up and configuration.

UNIT 5 MULTI BOARD COMMUNICATION 9

Multi Board Communication Software Design – Multi Board Architecture – Single control Card and Multiple line Card Architecture – Interface for Multi Board software – Failures and Fault – Tolerance in Multi Board Systems – Hardware independent development – Using a COTS Board – Development Environment – Test Tools.

L: 45 Total: 45 Hrs

REFERENCES

1. Sridhar .T, “Designing Embedded Communication Software” CMP Books, 2003.
2. Ahmed Amine Jerraya, Sungjoo Yoo, Diederix Veskest and Norbest Whn, “Embedded Software for SOC, Kulwar Academic Publishers, 2003.
3. Comer.D, ”Computer networks and Internet”, Third Edition, Prentice Hall, 2001.
4. T. Sridhar “Designing Embedded Communication Software”CMP Books, 2003.

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P13ESTE19 DSP INTEGRATED CIRCUITS

L	T	P	C
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UNIT 1 DSP INTEGRATED CIRCUITS AND VLSI CIRCUIT TECHNOLOGIES 9

Standard digital signal processors, Application specific IC's for DSP, DSP systems, DSP system design, Integrated circuit design. MOS transistors, MOS logic, VLSI process technologies, Trends in CMOS technologies.

UNIT 2 DIGITAL SIGNAL PROCESSING 9

Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal-processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT-The Fast Fourier Transform Algorithm, Image coding, Discrete cosine transforms.

UNIT 3 DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS 9

FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects -Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

UNIT 4 DSP ARCHITECTURES AND SYNTHESIS OF DSP ARCHITECTURES 9

DSP system architectures, Standard DSP architecture, Ideal DSP architectures, Multiprocessors and multicomputers, Systolic and Wave front arrays, Shared memory architectures. Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs.

UNIT 5 ARITHMETIC UNITS AND INTEGRATED CIRCUIT DESIGN 9

Conventional number system, Redundant Number system, Residue Number System. Bit-parallel and Bit-Serial arithmetic, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Layout of VLSI circuits, FFT processor, DCT processor and Interpolator as case studies.

L: 45 Total: 45 Hrs

REFERENCES

1. Lars Wanhammer, "DSP Integrated Circuits", 1999 Academic press, New York.
2. A.V.Oppenheim et.al, 'Discrete-time Signal Processing' Pearson education, 2000.
3. Emmanuel C. Ifeachor, Barrie W. Jervis, " Digital signal processing – A practical approach", Second edition, Pearson edition, Asia.
4. Keshab K.Parhi, 'VLSI digital Signal Processing Systems design and Implementation' John Wiley & Sons, 1999.

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P13ESTE20 INDUSTRIAL ROBOTICS AND EXPERT SYSTEMS

L	T	P	C
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UNIT1 ROBOTIC KINEMATICS AND DYNAMICS 9

Introduction to robotic kinematics- Definition, need and scope of industrial robot-Robot anatomy-Work volume-Precision movement-End effectors-Sensors, robot kinematics- Direct and inverse kinematics- Robot trajectories- Control of robot manipulations- Robot dynamics- Methods for orientation and location of objects.

UNIT2 ROBOT DRIVES AND CONTROL 9

Controlling the robot motion- Position and velocity sensing devices- Design of drivers of drives system- Hydraulic and pneumatic and linear and rotary actuators and control valves- Electro hydraulic servo valves, electric drives- Motors- designing of end effectors- Vacuum, magnetic and air operated grippers.

UNIT3 ROBOT SENSORS AND VISION SYSTEM 9

Transducers and sensors- Sensors in robot- Tactile sensor- Proximity and range sensors- Sensing joint forces- Robotic mission systems- Image gripping- image processing and image segmentation-Pattern recognition, training of vision system.

UNIT4 ROBOTIC CELL DESIGN AND APPLICATION 9

Robot work cell design and control- Safety in Robotics- Robot cell layouts- Multiple Robots and machine interference- Robot cycle time analysis- Industrial applications of robots.

UNIT5 ROBOT PROGRAMMING 9

Artificial Intelligence and expert systems- Methods of Robot programming- Characteristics of task level languages-Lead through programming methods- Motion interpolation- Artificial Intelligence-Basics- Goals of Artificial intelligence- AI Techniques-Problems- Representation in AI- Problems reduction and solution techniques- Application of AI and KBES in Robots.

L: 45 Total: 45 Hrs

REFERENCES

1. Fu, K.S., Gonzalez RC., and Lee C.S.G., "Robotics control, sensing, vision and intelligence," Mc Graw Hill, 1987.
2. Kozyrey, Yu."Industrial Robotics", Mir Publishers Mascow, 1985.
3. Deb.S.R, "Robotics Technology and Flexible Machine Design", Tata McGraw Hill 2005.\
4. Mikell.P.Groover, Michell Weis, Roger.N. Nagel, Nicolous G.Odrey,"Industrial Robotics Technology, Programming and Applications" McGraw Hill, Int,2005.
5. Timothy Jordonidess Etal, "Expert Systems and Robotics ", Springer- Verlager, Newyork, May 1991.
6. Richard D.Klafter, Thomas A.Chmielewski and Michael Negin, "Robotic Engineering: An Integrated Approach" Prentice- Hall of India, New Delhi, 2005.

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P13ESTE21 DATA COMMUNICATION AND NETWORKS

L	T	P	C
3	0	0	3

UNIT 1 INTRODUCTION TO NETWORK COMPONENTS 9

Components of network – Topologies – WAN / LAN – OSI – ISO layered Architecture Modulation and demodulation – Bit error rates – Line coding – Error correcting codes.

UNIT 2 DATA LINK LAYER 9

Design issues – CRC technique and sliding window techniques – Performance analysis of sliding window techniques – Framing formats – Case Study – HDLC protocols – Medium access control – CSMA / CD – Token ring and token bus – FDDI – Wireless LAN – Performance analysis of MAC protocols – Bridges.

UNIT 3 NETWORK LAYER 9

Circuit switching – packet switching – Design issues – IP addressing and IP diagram – Routers and gateways – Routing –Sub netting – CIDR – ICMP – ARP – RARP – Ipv6 – QoS.

UNIT 4 TRANSPORT LAYER 9

TCP and UDP – Error handling and flow control – Congestion control – TCP Retransmission – Timeout – Socket Abstraction.

UNIT 5 APPLICATION SERVICES 9

Simple Mail Transfer Protocol (SMTP) – File Transfer Protocols (FTP), telnet, the World Wide Web (WWW), Hypertext Transfer Protocol (HTTP), Domain name service (DNS), Security, Multimedia applications.

L: 45 Total: 45 Hrs

REFERENCES

1. William Stallings, “Data and Computer Communications”, Seventh Edition, Prentice Hall, 2003.
2. Larry Peterson, Bruce S Davie “Computer Networks: A Systems Approach”, Morgan Kaufmann Publishers, 2nd Edition, 1999.
3. James F Kurose, “Computer Networking: A Top – Down Approach Featuring the Internet”, Addison Wesley, 2nd Edition 2002.
4. W.Richard Stevens and Gary R Wright, “TCP / IP Illustrated”, Addison Wesley, Volume 1 & 2, 2001.
5. Douglas E Corner, “Internetworking with TCP / IP”, Volume 1 & 2, 2000.

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P13ESTE22	EMBEDDED CONTROL OF ELECTRICAL DRIVES	L	T	P	C
		3	0	0	3

UNIT1 MC68HC11 Microcontroller 9

Architecture memory organization – Addressing modes – Instruction set – Programming techniques – simple program.

UNIT2 PERIPHERALS OF MC68HC11 9

I/O ports – handshaking techniques – reset and interrupts – serial communication interface – serial peripheral interface – programmable timer – analog / digital interfacing – cache memory.

UNIT - III 8096 ARCHITECTURE 9

CPU operation – Interrupt structure – Timers – High Speed Input / Output Ports – I/O control and Status registers – Instruction Set – Addressing Modes – Simple Programming – Queues – Tables and Strings – Stack Memories – Key Switch – Parsing.

UNIT - IV PERIPHERALS AND INTERFACING 9

Analog Interface – Serial Ports – Watch dog timers – Real Time Clock – Multitasking – Bus Control – Memory Timing – External ROM and RAM expansion – PWM control – A/D interfacing.

UNIT - V CASE STUDY FOR MC68HC118051 AND 8096 9

Real Time clock – DC Motor Speed Control – Generation of Gating Signals for Converters and Inverters – Frequency Measurement – Temperature Control

L: 45 Total: 45 Hrs

REFERENCE:

1. John B.Peatman, “Design with Micro controllers”, McGraw Hill international Limited, Singapore, 2000.
2. Michael Slater, “Microprocessor based design A comprehensive guide to effective Hardware design” Prentice Hall, New Jersey, 2005.
3. Intel Manual on 16 bit embedded controllers, Santa Clara, 2000
4. Michael khevi, “The M68Hc11 Microcontroller Applications in Control, Instrumentation and Communication”, Prentice Hall, New Jersey, 2005.

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P13ESTE23 **MICROCONTROLLER BASED SYSTEM DESIGN**

L	T	P	C
3	0	0	3

UNIT I 8051 ARCHITECTURE 9

Architecture – memory organization – addressing modes – instruction set – Timers - Interrupts - I/O ports, Interfacing I/O Devices – Serial Communication.

UNIT II 8051 PROGRAMMING 9

Assembly language programming – Arithmetic Instructions – Logical Instructions –Single bit Instructions – Timer Counter Programming – Serial Communication Programming Interrupt Programming – RTOS for 8051 – RTOS Lite – Full RTOS –Task creation and run – LCD digital clock/thermometer using Full RTOS

UNIT III PIC MICROCONTROLLER 9

Architecture – memory organization – addressing modes – instruction set – PIC programming in Assembly & C –I/O port, Data Conversion, RAM & ROM Allocation, Timer programming, MP-LAB.

UNIT IV PERIPHERAL OF PIC MICROCONTROLLER 9

Timers – Interrupts, I/O ports- I2C bus-A/D converter-UART- CCP modules -ADC, DAC and Sensor Interfacing –Flash and EEPROM memories.

UNIT V SYSTEM DESIGN – CASE STUDY 9

Interfacing LCD Display – Keypad Interfacing - Generation of Gate signals for converters and Inverters - Motor Control – Controlling AC appliances –Measurement of frequency - Stand alone Data Acquisition System.

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L: 45 Total: 45 Hrs

REFERENCES:

1 Muhammad Ali Mazidi, Rolin D. Mckinlay, Danny Causey ‘ PIC Microcontroller and Embedded Systems using Assembly and C for PIC18’, Pearson Education 2008

2 John Iovine, ‘PIC Microcontroller Project Book ’, McGraw Hill 2000

3 Myke Predko, “Programming and customizing the 8051 microcontroller”, TataMcGraw Hill 2001.

4 Michael Slater, “Microprocessor based designs a comprehensive guide to effective Hardware design” Prentice Hall, New Jersey, 1989.

5 Ayala, Kenneth, “The 8051 Microcontroller” Upper Saddle River, New Jersey Prentice Hall, 2000.

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P13ESTE24 WIRELESS AND MOBILE COMMUNICATION

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UNIT 1 INTRODUCTION TO WIRELESS COMMUNICATION 9

Wireless Transmission-signal propagation-spread spectrum-Satellite Networks- Capacity Allocation-FAMA-DAMA-MAC

UNIT 2 MOBILE NETWORKS 9

Cellular Wireless Networks-GSM-Architecture-Protocols-Connection Establishment - Frequently Allocation-Routing-Handover-Security-GPRA

UNIT 3 WIRELESS NETWORKS 9

Wireless LAN-IEEE 802.11 Standard-Architecture-Services-Architecture of Ad. Hoc Network - HiperLan-Blue Tooth technology and its applications

UNIT 4 ROUTING 9

Mobile IP-DHCP- AdHoc Networks-Proactive and Reactive Routing Protocols with applications-features- Multicast Routing algorithms.

UNIT 5 TRANSPORT AND APPLICATION LAYERS 9

TCP over Adhoc Networks-WAP-Architecture-WWW Programming Model-WDPWTLS-WTP-WSP-WAE-WTA Architecture-WML-WML scripts.

L: 45 Total: 45 Hrs

REFERENCES

1 Kaveh Pahlavan, Prasanth Krishnamoorthy, " Principles of Wireless Networks' PHI/Pearson Education, 2003
2 Uwe Hansmann, Lothar Merk, Martin S. Nicklons and Thomas Stober, "Principles of Mobile computing", Springer, New york, 2003.
3 C.K.Toh, "AdHoc mobile wireless networks", Prentice Hall, Inc, 2002.
4 Charles E. Perkins, "Adhoc Networking", Addison-Wesley, 2001.
5 Jochen Schiller, "Mobile communications", PHI/Pearson Education, Second Edition, 2003.
6 William Stallings, "Wireless communications and Networks", PHI/Pearson Education, 2002.

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P13ESTE25 DSP FOR EMBEDDED SYSTEM

L	T	P	C
3	1	0	4

UNIT I SIGNALS AND REPRESENTATION 9

Classification of systems: Continuous, discrete, linear, causal, stable, dynamic, recursive, time variance; classification of signals: continuous and discrete, energy and power; mathematical representation of signals; spectral density; sampling techniques, quantization, quantization error, Nyquist rate, aliasing effect. Digital signal representation, analog to digital conversion.

UNIT II DISCRETE TIME SYSTEM ANALYSIS 9

Z-transform and its properties, inverse z-transforms; difference equation – Solution by z-transform, application to discrete systems - Stability analysis, frequency response – Convolution – Fourier transform of discrete sequence.

UNIT III DISCRETE FOURIER TRANSFORM & COMPUTATION 9

DFT properties, magnitude and phase representation - Computation of DFT using FFT algorithm – DIT & DIF - FFT using radix 2 – Butterfly structure.

UNIT IV DESIGN OF DIGITAL FILTERS 9

FIR & IIR filter realization – Parallel & cascade forms. FIR design: Windowing Techniques – Need and choice of windows – Linear phase characteristics. IIR design: Analog filter design - Butterworth and Chebyshev approximations; digital design using impulse invariant and bilinear transformation - Warping, prewarping - Frequency transformation.

UNIT V PROGRAMMABLE DSP CHIPS 9

Architecture and features of Black fin Processor - Real-Time DSP Fundamentals and Implementation Considerations - Memory System and Data Transfer - Code Optimization

L: 45 T: 15 Total: 60 Hrs

REFERENCE BOOKS

1. D.H. Hayes, 'Digital Signal Processing ', Schaum's Outline Series, Tata McGraw Hill, New Delhi, 2007.
2. B. Venkataramani, M. Bhaskar, 'Digital Signal Processors, Architecture, Programming and Applications', Tata McGraw Hill, New Delhi, 2003.
3. J.G. Proakis and D.G. Manolakis, 'Digital Signal Processing Principles, Algorithms and Applications', Pearson Education, New Delhi, 2003 / PHI.
4. Alan V. Oppenheim, Ronald W. Schafer and John R. Buck, 'Discrete – Time Signal Processing', Pearson Education, New Delhi, 2003.
5. Woon-Seng Gan, Sen.M. Kuo 'Embedded Signal Processing with the Micro Signal Architecture', John Willey Publications, 2006.

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P13ESTE26 **SOLID STATE CONVERTERS**

L	T	P	C
3	0	0	3

UNIT I SINGLE PHASE AC-DC CONVERTER 9

Uncontrolled, half controlled and fully controlled converters with R-L, R-L-E loads and free wheeling diodes – continuous and discontinuous models of operation – inverter operation – Dual converter - Sequence control of converters – performance parameters: harmonics, ripple, distortion, power factor – effect of source impedance and overlap.

UNIT II THREE PHASE AC-DC CONVERTER 9

Uncontrolled and fully controlled – converter with R, R-L, R-L-E - loads and free wheeling diodes – inverter operation and its limit – dual inverter – performance parameters – effect of source impedance and over lap

UNIT III DC-DC CONVERTERS 9

Principles of step-down and step-up converters – Analysis of buck, boost, buck-boost and Cuk converters – time ratio and current limit control – Full bridge converter – Resonant and quasi – resonant converters.

UNIT IV SINGLE PHASE INVERTERS 9

Principle of operation of half and full bridge inverters – Performance parameters – Voltage control of single phase inverters using various PWM techniques – various harmonic elimination techniques – forced commutated Thyristor inverters.

UNIT V THREE PHASE VOLTAGE SOURCE INVERTERS 9

180 degree and 120 degree conduction mode inverters with star and delta connected loads – voltage control of three phase inverters.

L: 45 Total: 45 Hrs

REFERENCES:

1. Ned Mohan, Undeland and Robbin, “Power Electronics: converters, Application and design” John Wiley and sons Inc, Newyork, 1995.
2. Rashid M.H., “Power Electronics Circuits, Devices and Applications ", Prentice Hall India, New Delhi, 1995.
3. P. C Sen.," Modern Power Electronics ", Wheeler publishing Co, First Edition, New Delhi-1998.
4. Jai P. Agrawal, “Power Electronics Systems”, Pearson Education, Second Edition, 2002.
5. P. S. Bimbra, “Power Electronics”, Khanna Publishers, Eleventh Edition, 2003.
6. Bimal K. Bose “Modern Power Electronics and AC Drives”, Pearson Education, Second Edition, 2003.

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